iSBX 352™
BIT SERIAL COMMUNICATIONS MULTIMODULE BOARD HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, preparation for use, programming information, principles of operation, and service information for the iSBC 352 Bit Serial Communication Multimodule Board. Supplementary information is provided in the following documents.

- *IBM Synchronous Data Link Control General Information,* IBM, GA27-3093-1.
- *Recommendation X.25,* ISO/CCITT March 2,1976.
- *System Network Architecture, Technical Overview,* IBM, GA 27-3102.
- *System Network Architecture Format and Protocol,* IBM, GA 27-3112.
- *Intel Peripheral Design Handbook.*
- *Intel Component Data Catalog*
- *Intel iSBX Bus Specification,* Order No. 9800683.
- *Intel Multibus Specification,* Order No. 142686.
- CCITT Standard for interfacing, CCITT-V.24.
- EIA Standard for RS232C Interfacing, EIA-RS-232C.
- EIA Standard for RS422 Interfacing, EIA-RS-422.
- EIA Standard for RS499 Interfacing, EIA-RS-449.

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CHAPTER 1
INTRODUCTION

1-1. INTRODUCTION

The iSBX 352 Bit Serial Communications Multimodule Board is a member of Intel's ever-expanding line of Multimodule board products designed to allow quick, easy, and inexpensive expansion of an Intel single board computer's functional capability. Contained on one single-wide iSBX form factor printed circuit board, the iSBX 352 board provides one channel of serial SDLC/HDLC communications protocol across either an RS232C or an RS422/449 interface. When configured for operation on an RS232C interface, the iSBX 352 board also meets the requirements of the CCITT V.24 interfacing standard. The Multimodule board attaches readily to any host iSBC board product that supports the iSBX Bus interface. In describing the iSBX 352 board, this manual presents the general information, preparation for use, programming, detailed theory of operation, and service information required for proper use of the board.

1-2. DESCRIPTION

The iSBX 352 Bit Serial Communications Multimodule Board, shown in Figure 1-1, provides, to any host iSBC microcomputer containing an Intel-standard iSBX Bus interface connector, a serial I/O channel that supports either HDLC or SDLC protocol on either an RS232C or RS422/449 standard interface. The iSBX 352 board contains the following features:

* One programmable synchronous serial channel.
* Compatibility with two program selectable protocols; either High Level Data Link Communications (HDLC) or IBM-compatible Serial Data Link Communications (SDLC).
* Compatibility with EIA RS232C, RS422/449, and CCITT V.24 interfacing standards.
* Compatibility with Receive-only, Transmit-only, full-duplex, and half-duplex operation.

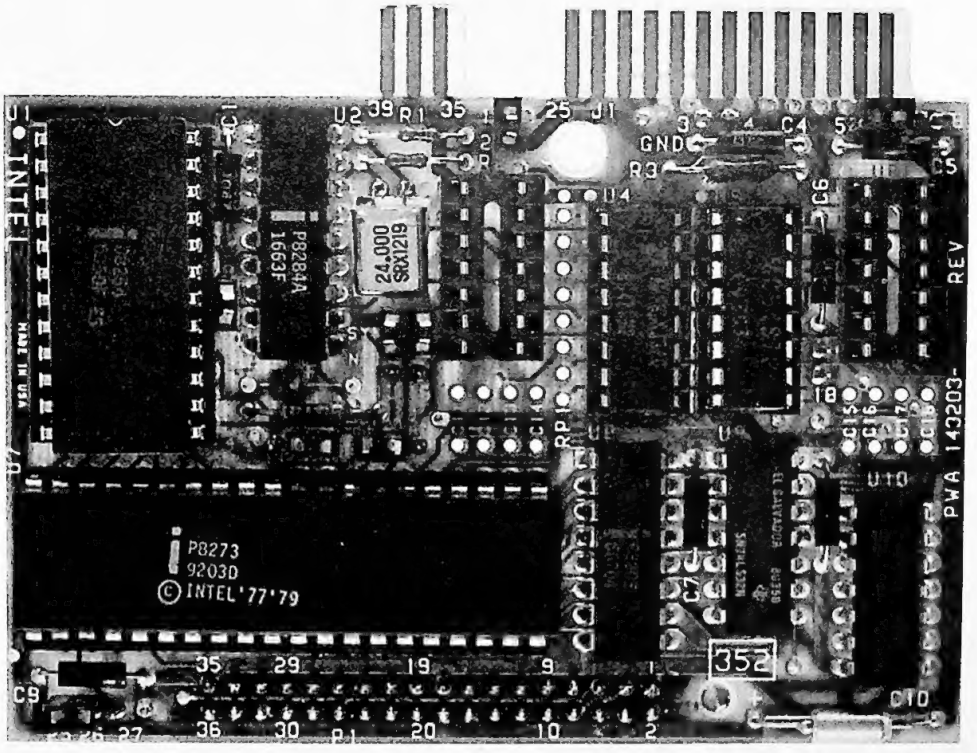


Figure 1-1. iSBX 352™ Bit Serial Communications Multimodule Board

* Selectable synchronous data transfer rates up to 48k bits per second (Note: 64k bps can be achieved under certain conditions).
* Self-clocking asynchronous data transfer rates up to 9.6k bits per second.
* Jumper selectable NRZI encoding/decoding and Phase-locked Loop clock recovery features on the serial channel.
* Data transfer coordination for base board via either interrupts or polling.
* Configuration as a Data Terminal Equipment (DTE) interface device.

The iSBX 352 board is designed to function in the iSBX environment complying with the iSBX Bus Specification. In doing so, the board performs 8-bit data transfer operations at a maximum rate of 48k bits per second.

1-3. EQUIPMENT SUPPLIED

The iSBX 352 board is shipped with a current revision of the schematic and two packaged RS232C line driver/receiver devices that may be installed as per instructions in Chapter 2 of this manual. As a member of the Intel Multimodule board family, the iSBX 352 board requires certain mounting hardware for installation on to a host iSBC micrcomputer board. The mounting hardware included with the board is as follows:

* 1 ea. Plastic mounting spacer
* 2 ea. Plastic mounting screws

1-4. SPECIFICATIONS

Table 1-1 lists the specifications and requirements for the iSBX 352 Bit Serial Communications Multimodule Board.

Table 1-1. Specifications

POWER REQUIREMENTS:	
RS232C Configuration	+5V ± .25V at 593 milliamps, −12V ± 0.6V at 28 milliamps, +12V ± 0.6V at 28 milliamps
RS422/449 Configuration	+5V ± .25V at 773 milliamps
ENVIRONMENTAL SPECIFICATIONS:	
Operating Temperature:	0 to 55° C (32 to 130° F)
Operating Humidity:	To 90% (without condensation)
COMMUNICATIONS INTERFACES:	The iSBX 352 board is compatible with the RS232C Interface Standard, the RS422/449 Interface Standard, and the CCITT V.24 Standard.
COMMUNICATIONS PROTOCOLS:	The iSBX 352 board supports a subset of the HDLC and SDLC communications protocols as defined in the following documents: *IBM Synchronous Data Link Control General Information*, IBM, GA 27-3093-1. *System Network Architecture, Technical Overview*, IBM, GA 27-3102. *System Network Architecture Format and Protocol*, IBM, GA 27-3112.
DATA TRANSMISSION OPERATION:	The iSBX 352 board supports Transmit-only operation, Receive-only operation, and half-duplex or full-duplex data transfer schemes.
OPERATING SPEEDS:	24 Mhz on-board crystal. 8 MHz clocking of the 8254-2 PIT. 4 MHz clocking of the 8273 device.
DATA THROUGHPUT SPEED:	64k bits per second (maximum). 48k bits per second if issuing commands during transmit operations.
PHYSICAL CHARACTERISTICS:	
Width	7.27 cm (2.85 inches)
Length	9.40 cm (3.70 inches)
Thickness	1.40 cm (0.56 inch)
Weight	72 gm (2.53 ounces)

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for preparing the iSBX 352 Bit Serial Communications Multimodule Board for use in a user-defined environment. Included in this chapter are instructions on unpacking and inspection; installation considerations such as power, cooling, size, and mounting requirements; user-provided component installation; jumper configuration; cabling requirements; and board installation information. It is advisable that the contents of Chapters 1 and 3 be fully understood before beginning the configuration and installation procedures contained in this chapter.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use in the event that the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, physical size, user provided components, and interfacing requirements are outlined in the following paragraphs.

2-4.POWER REQUIREMENTS

The power requirements for the iSBX 352 board vary depending on the type of interface required from the board. As Table 2-1 shows, the RS422/449 interface requires more current for operation.

2-5. COOLING REQUIREMENTS

The heat dissipation for the iSBX 352 board varies with the configuration of the board; Table 2-1 shows the maximum power dissipation for each configuration. Adequate circulation of air must be provided to prevent a temperature rise above 55° (131°). The system chassis units available from Intel include fans that provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

The outside dimensions of the iSBX 352 board are as follows:

a. Width: 7.27 cm (8.85 inches)
b. Length: 9.40 cm (3.70 inches)
c. Thickness: 1.40 cm (0.56 inch) Multimodule board only
2.82 cm (1.13 inch) Multimodule board and iSBC board.

Table 2-1. Power Requirements

Interface Configuration	Voltage Requirement	Current Requirement	Total Power Requirement	Heat (max.)
RS232C	+5.25 Volts −12.6 Volts +12.6 Volts	.593 Amp .028 Amp .028 Amp	3.8 Watts	54.38 gc/m (0.22 BTU)
RS422	+5.25 Volts	.773 Amp	4.1 Watts	57.79 gc/m' (0.23 BTU)

NOTE: All current, voltage, and heat figures are maximum.

2-7. USER-FURNISHED COMPONENTS

Table 2-2 lists all of the user provided components for configuring the iSBX 352 board to every intended configuration. Included in the table are names of manufacturers and their part numbers; any functionally and physically equivalent parts may be substituted.

RISE-TIME CAPACITORS. Normally the iSBX 352 board operates without installation of rise-time capacitors. However, in some RS232C applications, the rise-time speed of signals, fall-time speed of signals, or noise crosstalk must be controlled; this is perfomed by installing user provided rise-time capacitors onto the iSBX 352 board. Actual values of the capacitors are dictated by the configuration of each application. Most applications will not require installation of these capacitors.

Table 2-2 is a list of compatible capacitors for the iSBX 352 board and a cross reference list of various manufacturers. The capacitors must be installed into the eight locations labeled C11 through C18; refer to Figure 2-1 for the approximate location of the mounting holes on the board.

TERMINATION RESISTORS. In some RS422 applications, the Multimodule board may require an optional user provided termination resistor pack (SIP) to allow proper termination of the signal lines on the interface. Actual resistor values are dictated by the requirements of the application; refer to Appendix A for instructions on figuring the proper resistor size for the application.

Table 2-2 contains a list of compatible resistor SIPs (single in-line packs) for the iSBX 352 board and a cross reference list of various manufacturers. The 8-resistor SIP must be installed into the location labeled RP1; refer to Figure 2-1 for an approximate location.

FUSE. The iSBX 352 board can be configured to provide +5V power to the J1 connector at pin-23. Whenever the +5V power is provided to an off-board device, install a fuse onto the iSBX 352 board in the mounting position labeled F1; refer to Figure 2-1 for an approximate location. Table 2-2 contain the name of the manufacturer of a compatible fuse and a part number.

CAUTION

Ensure that the current drawn from the iSBX 352 board does not exceed 500 milliamps. Failure to do so could cause damage to the board.

LINE DRIVERS. As shipped, the iSBX 352 board is configured for operation with an RS422 interface. If reconfiguration to an RS232C interface is required, remove the 3486 and 3487 (RS422 interface) line drivers at chip locations U4 and U5 and install a provided 1488 (RS232C interface) line driver into the socketed chip location U6 and a provided 1489 (RS232C interface) line driver into the socketed chip location U3.

CAUTION

Ensure that only one set of line driver devices is installed into the iSBX 352 board; either the 3486/3487 devices at U4/U5 (respectively) or the 1488/1489 devices at U6/U3 (respectively). Failure to do so could cause damage to the iSBX 352 board.

Table 2-2. User Furnished Components

Component Type	Mfgr. Part No.		Mfgr. Names	Quantity	Comments
Rise/Fall-Time Capacitors	CKR05, CKR06		ACI, Inc. West Cap, Inc.	up to 8	2 pin packages; all standard capacitor values available; required only in RS232C or CCITT V.24 applications.
Terminating Resistor Pack (SIP)	608-3 764-3 4308-R-102 MSP08A03		TRW Beckman Bourns Dale	one	8-pin isolated resistor pack; all standard resistor values available; required only for RS422/449 applications.
Fuses	Amperage 0.5	Stock No. 27F1074	Type No. 276.500	one	All part numbers are from Littlefuse, Inc.; required if providing +5 volt power to an off-board application.

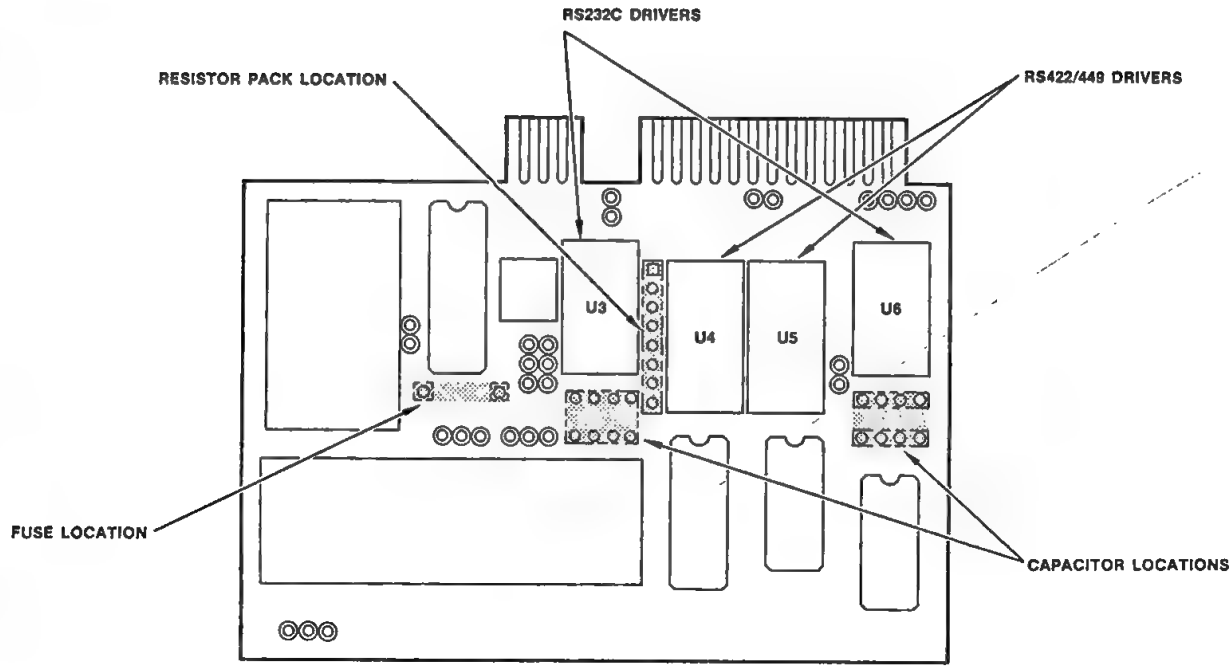


Figure 2-1. Component Location Drawing

CABLE/CONNECTORS. The user provided cables and connectors for interfacing connector J1 to the user environment will vary according to the type of interface required; i.e., whether RS232C or RS422/449. An RS422/449 interface requires a 40-pin edge connector (for J1), a 37-conductor cable, and a 37-pin RS449 standard connector. An RS232C interface requires a 26-pin edge connector (for J1), a 25-conductor cable, and a 25-pin RS232C standard connector. Recommended cable and connector manufacturers and their part numbers are presented later in this chapter. Notice that the Terminal Timing (TT) signal for an RS422/449 interface is provided on non-standard pins (pin-21 [B] and pin-3 [A]). More cabling information is contained in the interface configuration section of this chapter.

2-8. JUMPER CONFIGURATIONS

The iSBX 352 board contains 27 jumpers posts that may be user configured. Table 2-3 lists the functions performed by the jumpers and the various configurations for each. The "as-shipped" jumper configuration is shown in the table with asterisks.

2-9. iSBX BUS INTERFACE SPECIFICATIONS

The iSBX 352 board is designed for installation into a standard Intel iSBX Bus Connector. As shown in Figure 1-1, the iSBX Bus connector is a 18/36-pin connector (P1) that connects the iSBX 352 board to the iSBX Bus interface on a host iSBC microcomputer. Table 2-4 lists the pin assignments for the connector and Table 2-5 lists a description of the function of each signal. The dc characteristics of the signals on the connector are listed in Table 2-6.

2-10. SERIAL INTERFACE SPECIFICATIONS

The iSBX 352 board is designed to provide serial I/O capability via the J1 connector. As shown in Figure 1-1, the J1 connector is a 26/40-pin connector that provides interfacing to a remote resource via either an RS232C or an RS422/449 interface. Table 2-7 lists the pin assignments for the J1 connector (both RS232C and RS422/449) and Table 2-8 contains descriptions of the functions of each RS232C and RS422/449 signal. Connector information is provided later in this chapter.

Table 2-3. Jumper Configurations

Jumper Number	Configuration	Function
E1-E2*	RS422/449	Provides the Send Common (SC) signal on pin-35 of connector J1.
E3-E4	RS232C	Provides the Signal Ground (SGND) on pin-14 of connector J1.
E5-E6*	RS422/449	Provides the Receive Common (RC) signal on pin-1 of connector J1.
E7-E8	RS232C	Provides the Frame Ground (FG) on pin-2 of connector J1.
E9-E10*	All	Enables the on-board 8 MHz clock from the 8284A clock generator to drive the 8254-2 PIT.
E11,E12,E13		8273 Transmit Clock Selection
E11-E12	SYNC	Synchronous operation; disables the 32x Clock to the 8273 device.
E12-E13*	NRZI	Self-clocking operation; enables the 32x Clock for the digital phase Lock Loop on the 8273.
E14,E15,E16		8273 Receive Clock Selection
E14-E15	SYNC	Synchronous operation; selects the Receive Clock for the 8273 from the serial interface.
E15-E16*	NRZI	Self-clocking operation; selects the Receive Clock for the 8273 from the internal digital phase Lock Loop.
E17-E18	Multidrop	Required for operation in a multidrop application; enables the Data Terminal Ready (DTR) signal to control the tri-stating of the RS422 drivers.
E19,E20,E21	All	CTS signal control.
E19-E20		Connected when the iSBX 352 board is a master in either a Multidrop or a loop configuration to disable the Clear To Send (CTS) signal.
E20-E21*		Connected when the iSBX 352 board is operating as a slave device in the Multidrop or loop configuration requiring the CTS signal.
E22,E23,E24	All	Transmit Clock selection.
E22-E23*		Connected for normal transmit clock generation (via the bit rate generator).
E23-E24		Connected to generate the transmit clock (TxC) from the receive data via the digital phase lock loop (DPLL) circuitry in the 8273.
E25,E26,E27	All	Enables either a timer signal or a service request signal to an off-board resource via the OPT0 line.
E25-E26*		Enables the Receiver Service Request signal.
E26-E27		Enables the OUT2 clock from the 8254 PIT.

*Configured As-shipped.

Table 2-4. iSBX™ Bus Connector (P1) Pin Assignment

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	SIGNAL GROUND	36	+5V	+5 Volts
33	MD0	MDATA BIT 0	34	—	Reserved
31	MD1	MDATA BIT 1	32	—	Reserved
29	MD2	MDATA BIT 2	30	OPT0	OPTION 0
27	MD3	MDATA BIT 3	28	OPT1	OPTION 1
25	MD4	MDATA BIT 4	26	—	Reserved
23	MD5	MDATA BIT 5	24	—	Reserved
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20	MCS1/	M CHIP SELECT 1
17	GND	SIGNAL GROUND	18	+5V	+5 Volts
15	IORD/	IO READ COMMAND	16	—	Reserved
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12	MINTR1	M INTERRUPT 1
9	MA1	M ADDRESS 1	10	—	Reserved
7	MA2	M ADDRESS 2	8	MPST/	M PRESENT
5	RESET	RESET	6	—	Reserved
3	GND	SIGNAL GROUND	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Table 2-5. iSBX Bus Connector Signal Description

SIGNAL NAME	DESCRIPTION
RESET (Reset)	This active HIGH signal, when asserted to the iSBX 352 board via connector P1 pin-5, holds the 8273 device on the iSBX 352 board in an idle state.
MD0-MD7 (Bidirectional data bus)	These eight, active HIGH, bidirectional data lines provide a means of transferring commands, parameters, status, and data between the LSI devices on the iSBX 352 board (8273 and 8254-2 PIT) and the CPU on the host iSBC microcomputer.
IORD/ (Read Command)	This active LOW input signal to the iSBX 352 board is generated by the host iSBC microcomputer as a command to the iSBX 352 board to output either data or status via the bidirectional data bus (MD0-MD7) to the host iSBC microcomputer.
IOWRT/ (Write Command)	This active LOW input signal to the iSBX 352 board is generated by the host iSBC microcomputer as a command to the iSBX 352 board to accept data present on the bidirectional data bus.
MCS0/ and MCS1/ (Chip Selects)	These active LOW input signals to the iSBX 352 board enable the response to either an input or an output instruction executed on the host iSBC microcomputer board.
MA0, MA1, MA2 (Function Selectors)	These active HIGH inputs from the host iSBC microcomputer select the register in the 8273 that is to be accessed during the operation performed on the iSBX 352 board.
OPT0 (Receiver Data Transfer Request or PIT Counter 2 Output)	This active HIGH output signal from the 8273 device on the iSBX 352 board provides an indication to the host iSBC microcomputer that the receive logic within the 8273 device requires data transfer service.
OPT1 (Transmitter Data Transfer Request)	This active HIGH output from the iSBX board provides the Transmitter Data Transfer Request signal from the 8273 device to the host iSBC microcomputer.
MINTR0 (Transmitter Interrupt)	This active HIGH output from the 8273 device on the iSBX 352 board provides the host iSBC microcomputer with an interrupt request signal whenever the transmitter portion of the 8273 requires service.
MINTR1 (Receiver Interrupt)	This active HIGH output from the 8273 device on the iSBX 352 board provides the host iSBC microcomputer with an interrupt request signal whenever the receiver portion of the 8273 requires service.

Table 2-6. AC and DC Signal Characteristics for iSBX Bus Connector

Output Signal Name	Type[2] Drive	I_{OL} Max -Min (mA)	@ Volts (V_{OL} Max)	I_{OH} Max -Min (μA)	@ Volts (V_{OH} Min)	C_O (Min) (pf)
MD0-MD7	TRI	1.6	0.5	-200	2.4	130
MINTR0-1	TTL	2.0	0.5	-100	2.4	40
MDRQT	TTL	1.6	0.5	- 50	2.4	40
MWAIT/	TTL	1.6	0.5	- 50	2.4	40
OPT1-2	TTL	1.6	0.5	- 50	2.4	40
MPST/	TTL	Note[1]				
Intput Signal Name	**Type[2] Receiver**	**I_{IL} Max (mA)**	**@ V_{IN} Max (volts)**	**I_{IH} Max (μA)**	**@ V_{IN} Max (volts)**	**C_I Max (pf)**
MD0-MD7	TRI	-0.5	0.8	70	2.0	40
MA0-MA2	TTL	-0.5	0.8	70	2.0	40
MCS0/-MCS1/	TTL	-4.0	0.8	100	2.0	40
MRESET	TTL	-2.1	0.8		2.0	40
MDACK/	TTL	-1.0	0.8	100	2.0	40
IORD/ IOWRT/	TTL	-1.0	0.8	100	2.0	40
MCLK	TTL	-2.4	0.8	100	2.0	40
OPT1-OPT2	TTL	-2.0	0.8	100	2.0	40

NOTES:
1. iSBX Multimodule board must connect this signal to ground.
2. TTL = standard totem pole output. TRI = Three-state

Table 2-7. J1 Connector Pin Assignments

J1 Connector Pin	RS232C Connector Pin	iSBX 352™ Support	RS232 Name	RS232 Function	RS422 Connector Pin	iSBX 352™ Support	RS449 Name	RS449 Function
1	14	—	(S) TXD	Secondary Transmit Data	20	YES	RC	Receive Common
2	1	YES	FG	Frame Ground	1	YES	Shield	Shield
3	15	—	DCE TXC	Transmit Clock	21*	YES	Spare	Terminal Timing (TT)
4	2	YES	TXD	Transmit Data	2	—	SI (A)	Signaling Rate Indicator
5	16	—	(S) RXD	Secondary Receive Data	22	YES	SD (B)	Send Data
6	3	YES	RXD	Receive Data	3*	YES	Spare (B)	Terminal Timing (TT)
7	17	YES	RXC	Receive Clock	23	—	ST (B)	Send Timing
8	4	YES	RTS	Request To Send	4	YES	SD (A)	Send Data
9	18	—	—	—	24	YES	RD (B)	Receive Data
10	5	YES	CTS	Clear To Send	5	—	ST (A)	Send Timing
11	19	—	(S) RTS	Secondary Request To Send	25	YES	RS (B)	Request To Send
12	6	YES	DSR	Data Set Ready	6	YES	RD (A)	Receive Data
13	20	YES	DTR	Data Terminal Ready	26	YES	RT (B)	Receive Timing
14	7	YES	SG	Signal Ground	7	YES	RS (A)	Request To Send
15	21	—	SQ	Signal Quality	27	YES	CS (B)	Clear To Send
16	8	—	DCD	Data Carrier Detect	8	YES	RT (A)	Receive Timing
17	22	—	RI	Ring Indicator	28	—	IS (A)	In Service
18	9	—	—	—	9	YES	CS (A)	Clear To Send
19	23	—	CH/CI	Signaling Rate Indicator	29	YES	DM (B)	Data Mode
20	10	—	—	—	10	—	LL (A)	Local Loopback
21	24	YES	DTE TXC	Transmit Clock	30	YES	TR (B)	Terminal Ready
22	11	—	—	—	11	YES	DM (A)	Data Mode
23	25	*	—	+5V Power	31	—	RR (B)	Receiver Ready
24	12	—	(S) DCD	Secondary Data Carrier Detect	12	YES	TR (A)	Terminal Ready
25	N/C	—	—	—	32	—	SS (A)	Select Standby
26	13	—	(S) CTS	Secondary Clear To Send	13	—	RR (A)	Receiver Ready
36	N/C				37	YES	SC	Send Common
36	N/C				18	—	TM (A)	Test Mode
37	N/C				N/C	—	—	—
38	N/C				19	YES	SG	Signal Ground
39	N/C				N/C	—	—	—
40	N/C				N/C	—	—	—

NOTES:
* Non-standard usage of this line

Table 2-8. J1 Connector DC Specifications

Connector J1 Signal	Parameter	Test Conditions	Min.	Max.	Units
RS232C Input	Input High Threshold		1.75	+8.30	V
	Input Low Threshold		-0.75		V
	Input Current	V_{IN} = +25V		+8.30	mA
		V_{IN} = -25V		-8.30	mA
RS232C Output	High Output Voltage	R_L = 3K ohms	7.7	—	V
	Low Output Voltage		-7.7	—	V
	High Short Circuit Current	V_{AA}, V_{DD} = min.	-8.0	-16.0	mA
	Low Short Circuit Current		8.0	16.0	mA
RS422 Input	Input High Threshold (Differential)		—	0.2	V
	Input Low Threshold (Differential)		—	-0.2	V
	Input Current	V_{IN} = +3V	—	+1.5	mA
		V_{IN} = -3V	—	-1.5	mA
		V_{IN} = +10V	—	+3.25	mA
		V_{IN} = -10V	—	-3.25	mA
	Input Common Mode		—	±15.0	V
	Input Differential		—	±15.0	V
RS422 Output	High Out Voltage	I_{OH} = -20mA	2.5	—	V
	Low Out Voltage	I_{OL} = 20mA	—	0.5	V
	Short Circuit Current	V_{CC} = max.	-30	-150	mA
	High Output Leakage Current (Power Off)	V_{OH} = 6.0V V_{CC} = 0.0V	—	+100.00	μA
	Low Output Leakage Current (Power Off)	V_{OL} = -0.25V V_{CC} = 0.0V	—	-100.0	μA
	High or Low Output Leakage Current (High Impedance Condition)			±100.0	μA
	DTRD Current	V_{OH} = 2.0V min. V_{OL} = 0.8V max.		100.0 -2.0	μA mA
	Buffer Control Current	V_{OH} = 2.0V min. V_{OL} = 0.8V max.		20.0 -1.2	μA mA

2-11. DATA LINK INTERFACE CONFIGURING OPTIONS

Some data link configuration examples for the iSBX 352 Bit Serial Communication Multimodule Board are shown in Figures 2-2, 2-3, 2-4, 2-5, and 2-6, and described in the following paragraphs. In addition to the configuration information, some of the communications terms are defined in Table 2-9. More information on the various types of data links is available in the *IBM Synchronous Data Link Control, General Information* manual as listed in the preface.

The iSBX 352 board provides six interfacing options for the serial data link interface (connector J1). To summarize, the five basic data link configurations available for the iSBX 352 Bit Serial Communications Multimodule Board are as follows:

* Half-duplex, multidrop, non-switched,
* Full-duplex, multidrop, non-switched,
* Full-duplex, point-to-point, non-switched,
* Half-duplex, point-to-point, non-switched,
* Half-duplex, point-to-point, switched, and
* Half-duplex, loop.

Each type of data link configuration requires different jumper connections on the iSBX 352 board. The jumpers on the iSBX 352 boards must be configured as listed in the table included with each configuration. The J1 interface consists of both dedicated and user defined modem control signals that are active LOW. The J1 connector interface may be implemented with either the RS232C or the RS422/449 interface standard, however, a multidrop configuration requires an RS422/449 interface for proper operation.

In addition to the basic data link configuring options, the iSBX 352 board allows the option of selecting either self-clocked or synchronous clocked data transfer operation. The following five paragraphs provide an overview and a picture for five of the many data link configurations, including; synchronous point-to-point operating mode, a self-clocking point-to-point operating mode, a synchronous multidrop operating mode (with modems), a self-clocking operating mode, and a self-clocking SDLC Loop Network configuration. Each of these configurations is described in the following paragraphs and shown in Figures 2-2, 2-3, 2-4, 2-5, and 2-6.

2-12. SYNCHRONOUS MODE INTERFACE WITH MODEM. Figure 2-2 shows the synchronous mode interface operation of the iSBX 352 board for an RS232C interface. The RS422/449 application would include two conductors for each interface signal; one for the positive and one for the negative signal polarity. The RS232C application, on the other hand, requires only one conductor per interface signal. The figure describes connection of a modem configuration; a non-modem configuration is also available, if required.

The synchronous mode of operation requires a modem for generation of the receive clock (RxC) for coordination of the data transfer. The iSBX 352 board generates the transmit synchronizing clock (TxC) during synchronous mode operations.

2-13. SELF-CLOCKING MODE INTERFACE WITH MODEM. Although the iSBX 352 board is compatible with the HDLC/SDLC communication line protocols, which are primarily designed for synchronous data communication, the iSBX 352 board can be use in an asynchronous mode interface when configured as shown in Figure 2-3. The option of using or not using a modem is available for both RS232C and RS422/449 interfacing applications.

The self-clocking mode interface employs the digital phase lock loop (DPLL) feature of the on-board 8273 for clock recovery and programmable NRZI encoding/decoding (another 8273 feature) of data. The use of NRZI encoding with an SDLC transmission scheme ensures that a transition will occur on the data line at least once every five bit-times during a frame transmission; i.e., the longest allowable sequence without a transition (and without zero insertion) will

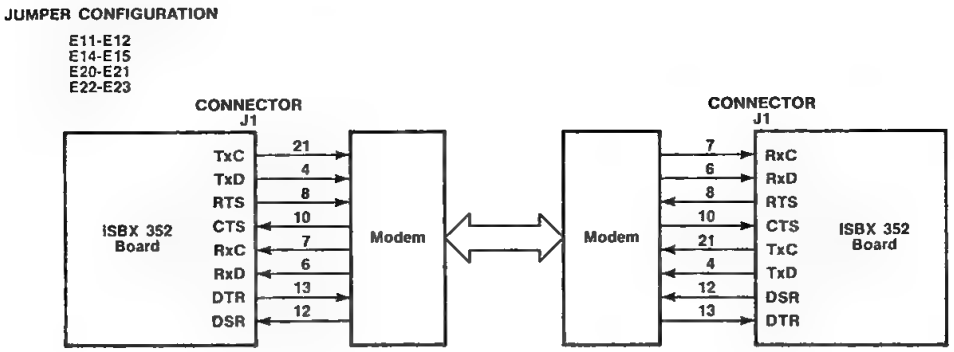


Figure 2-2. Synchronous Point-to-Point Modem Interface Configuration Example-RS232C

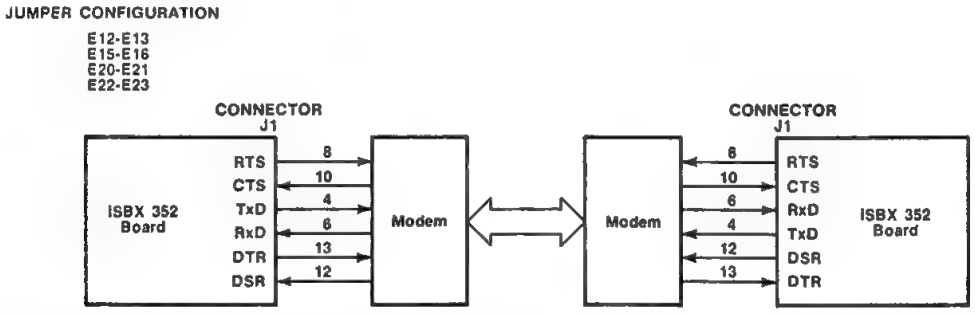


Figure 2-3. Self-Clocking Point-to-Point Modem Interface Configuration Example-RS232C

be five bit times. The digital phase lock loop allows operation of the interface in either a half-duplex or a full-duplex implementation with or without modems. The 8254-2 PIT must be configured for operation at a speed that is 32 times that of the data rate.

2-14. MULTIDROP NETWORKING APPLICATION (Synchronous.) Figure 2-4 shows a typical synchronous multidrop application. In a Multidrop application, the iSBX 352 board must be operating with an RS422/449 interface so that the non-participating units can be tri-stated. In Figure 2-4, each signal line represents a cable pair; the B portion of the signal is found on the pin number listed in the parenthesis.

2-15. MULTIDROP NETWORKING APPLICATION (Self-Clocking). Figure 2-5 shows a typical self-clocking multidrop application. In a multidrop application, the iSBX 352 board must be operating with an RS422/449 interface so that the non-participating units can be tri-stated. In Figure 2-5, each signal line represents a cable pair; the B portion of the signal is found on the pin number listed in the parenthesis.

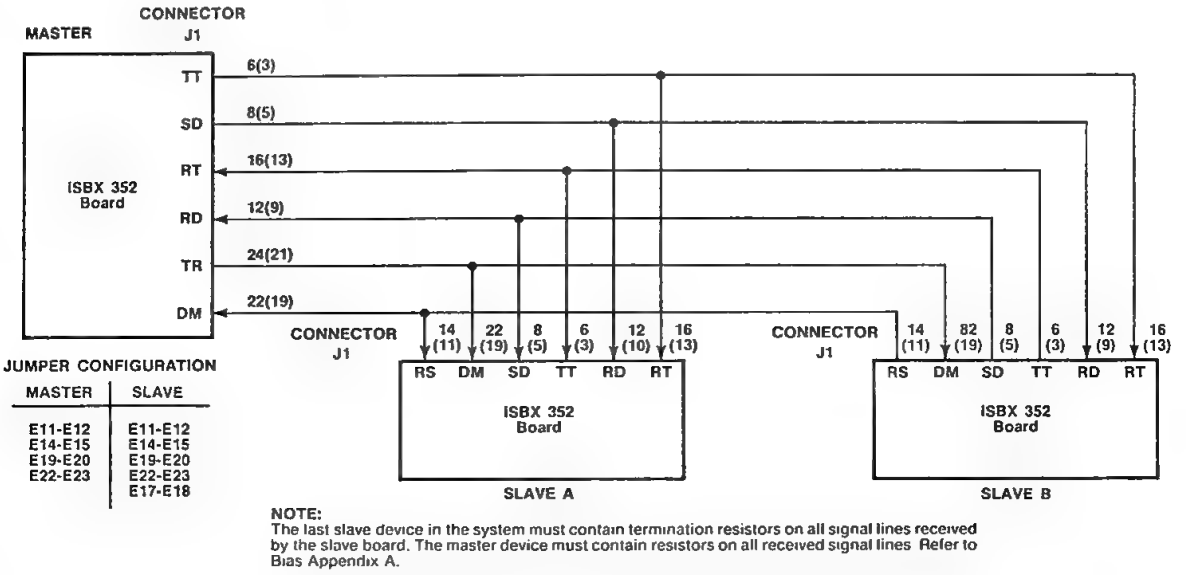


Figure 2-4. Synchronous Multidrop Network Configuration Example - RS422

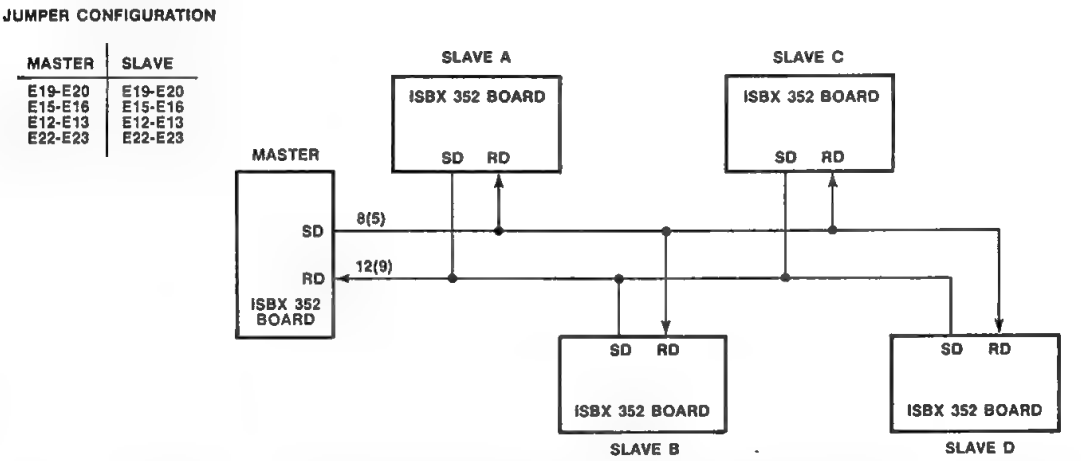


Figure 2-5. Self-Clocking Multidrop Configuration Example - RS422

2-16. SDLC LOOP NETWORK APPLICATION (either Self-Clocking or Synchronous). The SDLC Loop network application is shown in Figure 2-6. In an SDLC loop network application, the iSBX 352 board may require operation with an RS422/449 interface; an RS232C interface does not provide the required drive capability when operating over long cable lengths.

Implementation of the SDLC loop network application is greatly simplified by the digital phase lock loop feature of the 8273 device on the iSBX 352 board. In this mode of operation, each secondary station on the loop is considered to be a repeater set in one-bit-delay mode. The data sent out by the primary station (the loop controller) are relayed bit-for-bit through each secondary station and finally, back to the primary station. The secondary station finding its address in the message begins to execute the command in the message while still passing the entire message along to the next secondary station. After the message is passed, the secondary station begins transmitting the data (if any) in the message. Notice that the loop controller requires a transmit clock and all secondary stations operate in the digital-phase-lock-loop mode while passing the message and data.

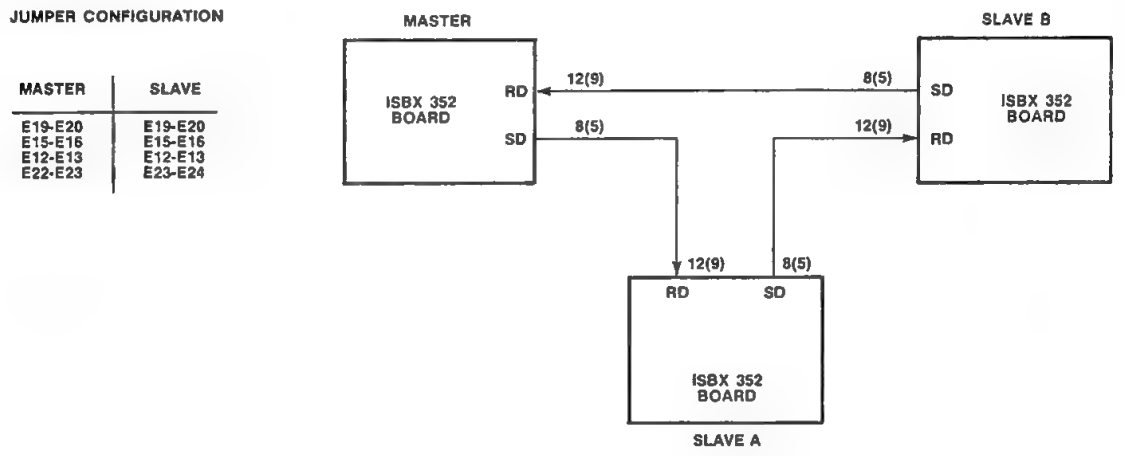


Figure 2-6. Self-Clocking SDLC Loop Network Configuration Example

Table 2-9. Term Definitions

Data Link	The data link consists of the data communication equipment (DCE), the data terminal equipment (DTE), and the data communication channel. Typically, the data link includes the circuitry for serializing the data, the circuitry for converting the data to signal levels compatible with voice-grade transmission equipment, and the circuitry for deserializing the data.
Point-To-Point, Multidrop, and Loop Networks	The iSBX 352 board may be used in three basic configurations; point-to-point multidrop, and loop. A point-to-point configuration is a data link with only two stations. A multidrop configuration is a data link with three or more stations on a serial non-looped bus. A loop configuration is a data link of three or more stations that pass the data among themselves sequentially in a loop.
Full-Duplex Half-Duplex Communication	In addition, both the point-to-point and the multidrop data link configurations can operate as either a half-duplex (two-way alternate) or a full-duplex (two-way simultaneous) communication channel.
Switched, Non-switched Communication	A point-to-point half-duplex channel may be either switched or non-switched. A non-switched channel is one that is permanently connected. A switched channel, on the other hand, is a temporary connection such as the connection made in placing a telephone call.

2-17. RS232C INTERFACE CONFIGURATION.

Configuration options available on the iSBX 352 board in an RS232C interface application include:

* Addition of rise/fall-time capacitors to control the rise and fall-times of the RS232C interface signals to control the crosstalk and
* Configuration of a user-provided I/O cable and connector assembly for either standard or non-standard RS232C interfacing on the J1 connector.

Refer to Table 2-2 for more information on the capacitors and to paragraph 2-20 for more information on the I/O cabling requirements.

2-18. RS422/449 INTERFACE CONFIGURATION

Configuration options available on the iSBX 352 board in an RS422/449 interface application include:

* Addition of termination resistors to properly terminate the RS422/449 interface signals, and
* Configuration of a user-provided I/O cable and connector assembly for either standard or non-standard RS449 interfacing on the J1 connector.

Refer to Table 2-2 for more information on the resistors and to paragraph 2-19 for more information on the I/O cabling configuration.

2-19. I/O CABLE CONFIGURATION

The user-provided I/O cable and connector requirements vary according to the type of interface in which the iSBX 352 board is applied. An RS232C interface application requires a 26-pin edge connector, a 25-conductor flat ribbon cable, and a 25-pin RS232C connector. An RS422/449 interface requires a 40-pin edge connector, a 37-conductor flat ribbon cable, and a 37-pin RS449 connector. Table 2-10 lists some recommended cable and connector part numbers and a manufacturer. Any functionally equivalent parts may be substituted.

When assembling the RS232C cable, ensure that pin-25 of the J1 edge connector is not connected to a conductor in the flat ribbon cable, and ensure that pin-1 of the RS232C interface connector on the flat ribbon cable is connected to pin-2 of the 26-pin edge connector and to pin-1 of the J1 connector on the board. Refer to Figure 2-7.

When assembling the RS422/449 cable, ensure that pins 37, 39, and 40 of the J1 edge connector are not connected to a conductor in the flat ribbon cable, and ensure that pin-1 of the RS449 interface connector on the flat ribbon cable is connected to pin-2 of the 40-pin edge connector and to pin-1 of the J1 connector on the board. Refer to Figure 2-8.

Figure 2-9 shows the pin numbering of both the iSBX 352 board edge connector (J1) and the connectors for the cable.

Table 2-10. Cabling Information

Configuration	Mode[2]	Multimodule Edge Connector	Cable	Connector
RC232C	DTE	26-pin[5], 3M-3462-0001	3M[3]-3349/25	25-pin[7], 3M-3482-1000
RS232C	DCE	26-pin[5], 3M-3462-0001	3M[3]-3349/25	25-pin[7], 3M-3483-1000
RS449	DTE	40-pin[6], 3M-3464-0001	3M[4]-3349/37	37-pin[1], 3M-3502-1000
RS449	DCE	40-pin[6], 3M-3464-0001	3M[4]-3349/37	37-pin[1], 3M-3503-1000

NOTES:
1. Cable housing 3M-3485-4000 may be used with the connector.
2. DTE - Data Terminal Equipment mode (male connector). DCE - Data Set Equipment mode (female connector).
3. Cable is tapered at one end to fit the 3M-3462 connector.
4. Cable is tapered to fit 3M-3464 connector.
5. Pin 26 of the edge connector is not connected to the flat cable.
6. Pins 38, 39, and 40 of the edge connector are not connected to the flat cable.
7. May be used with the cable housing 3M-3485-1000.

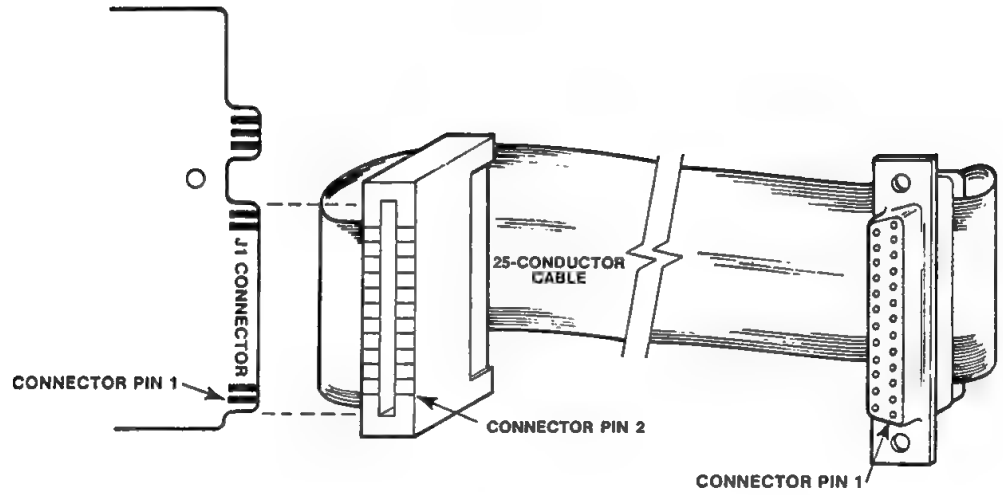


Figure 2-7. RS232C Interface Cabling

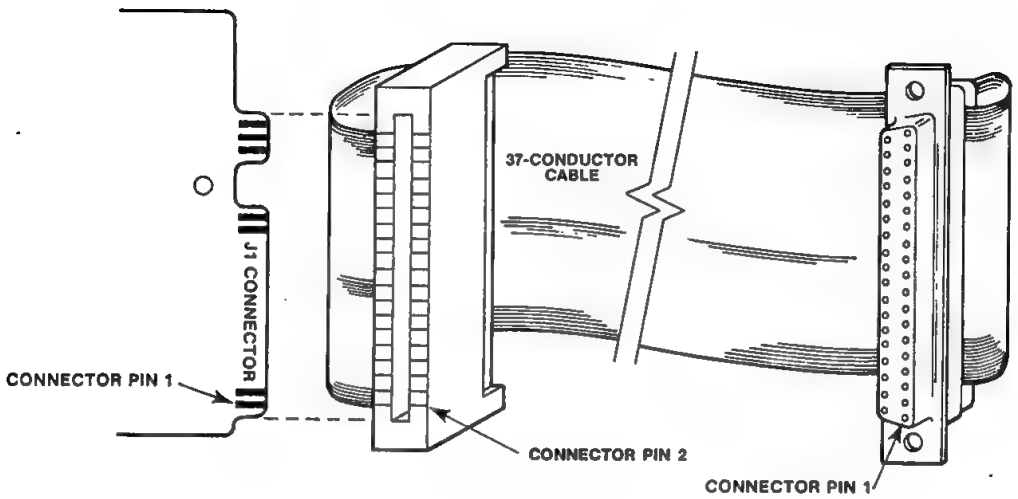


Figure 2-8. RS422/449 Interface Cabling

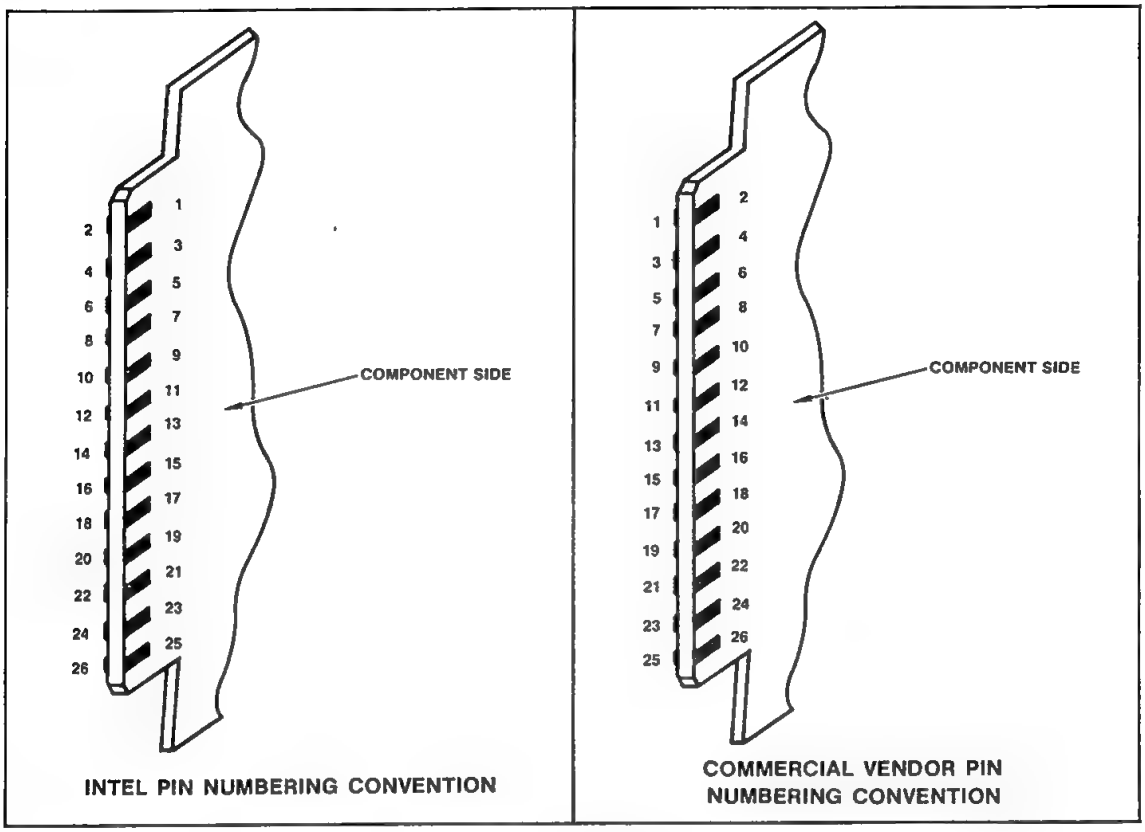


Figure 2-9. Connector Pin Numbering Comparison

2-20. BOARD INSTALLATION

The iSBX 352 board is shipped with mounting hardware required to fasten the Multimodule board to a host iSBC microcomputer board. Proceed as follows:

CAUTION

Always remove power from the boards when reconfiguring the system. Failure to do so could cause damage to the boards.

a. Locate the mounting hardware provided with the Multimodule board; two 6-32 plastic screws and one 1/2 inch threaded plastic spacer.

b. With one of the screws, secure the plastic spacer to the host iSBC microcomputer board as shown in Figure 2-10.

c. Locate pin-1 of the iSBX connector (P1) on the Multimodule board and align it with pin-1 of the iSBX connector on the host iSBC microcomputer board.

d. Gently, press the Multimodule board onto the host iSBC microcomputer board until the connectors are mated properly.

e. Align the mounting hole on the Multimodule board with the hole in the top of the plastic spacer.

f. Fasten the Mulitmodule board to the spacer with the other plastic screw provided.

NOTE

The final position of a Multimodule board installed onto a host iSBC microcomputer may vary according to the type of host iSBC microcomputer used.

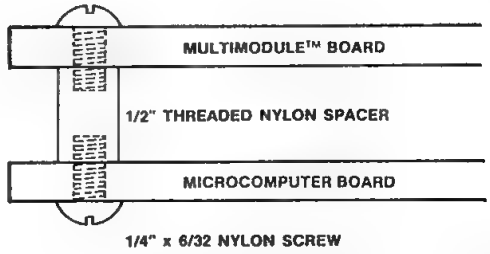


Figure 2-10. Multimodule Board Installation

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter describes the programming required to use the iSBX Bit 352 Bit Serial Communication Multimodule Board in an RS232C or RS422/449 interfacing application. Included are sections on addressing, command formats, data selection formats, interrupt servicing, and programming examples.

3-2. COMMUNICATION PROTOCOL OVERVIEW

The communication protocol generated by the iSBX 352 Bit Serial Communications Multimodule Board is generally that of the 8273; that is, HDLC/SDLC communications standard protocol across either an RS232C or an RS422/449 interface. The iSBX 352 board must be interfaced to another RS232C or RS422/449 interface device that can accept HDLC/SDLC protocol and successfully decode the data. In programming the iSBX 352 board, a user should be familiar with the HDLC and SDLC protocol standards since the protocol formatting, encoding, and decoding required for generating HDLC/SDLC standard communications is performed internally within the 8273 Programmable HDLC/SDLC Protocol Controller as a result of commands issued to the 8273. A working understanding of the control and data interfacing requirements and status messages from the 8273 is required. The following paragraphs provide an overview of the HDLC/SDLC communication protocol.

FRAMES

The basic communication element in HDLC/SDLC protocol is called a FRAME. A frame can be used for both link control and data transfer purposes. The fields within a frame (refer to Figure 3-1) include an eight bit BEGINNING FLAG (F) consisting of one zero, six ones, and a zero; an eight bit ADDRESS FIELD (A); an eight bit CONTROL FIELD (C); a variable length (N-bit) INFORMATION FIELD (I); a sixteen bit FRAME CHECK SEQUENCE (FCS); and an eight bit END FLAG (F) with the same bit pattern as the beginning flag. In HDLC the Address (A) and Control (C) fields are extendable. The HDLC and the SDLC protocols use three types of frames; an Information Frame is used to transfer data, a Supervisory Frame is used for control purposes, and a Non-sequenced Frame is used for initialization and control of the secondary stations. More information on the various types of frames can be found in the SDLC Protocol Standard.

FRAME CHARACTERISTICS

An important characteristic of a frame is that its contents are made code transparent by use of a zero-bit insertion/deletion. Thus, the user can adapt the data transfer to any format or code suitable for his system. The frame is bit oriented; that is, bits rather than characters in each field have specific meanings. The Frame Check Sequence (FCS) character is a result of an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices.

The command and response frames of a typical communication sequence contain sequence numbers in their control fields identifying each frame. The sequence numbers are intended to be used in error recovery and as implicit acknowledgement of frame communication, a use that enhances the true full-duplex nature of the HDLC/SDLC protocols. In contrast, the BISYNC communications protocol is basically half-duplex (two way alternate) because of necessity to transmit immediate acknowledgement frames. HDLC/SDLC protocol has twice the potential throughput rate of the BISYNC protocol.

It is possible to use HDLC/SDLC protocol over half-duplex lines but there is a corresponding loss in throughput; both protocols are designed primarily for full-duplex communication. As in any synchronous system, the bit rate of the iSBX 352 board is determined by the clock supplied to the modem.

A byproduct of the use of zero-bit insertion/deletion performed by the 8273 in generating the HDLC/SDLC protocol is the non-return-to-zero invert (NRZI) data transmission/reception capability that it provides for the iSBX 352 board. The zero-bit insertion allows HDLC/SDLC protocols to be used with asynchronous data communication hardware in which the clocks are derived from the NRZI encoded data.

Figure 3-1 lists the Information field of a frame as being of variable length. The iSBX 352 board can receive a variable length Information field, but cannot transmit one.

BEGINNING FLAG	ADDRESS FIELD	CONTROL FIELD	INFORMATION FIELD (OPTIONAL)	FRAME CHECK SEQUENCE FIELD	ENDING FLAG
01111110	8 BITS	8 BITS	VARIABLE LENGTH	16 BITS	01111110

Figure 3-1. Typical SDLC Frame Format

3-3. ADDRESSING

The host iSBC microcomputer addresses an iSBX 352 board by using one of the valid port addresses as listed in Table 3-1. Since some host iSBC microcomputers will accept up to three Multimodule boards, the upper address byte for each iSBX bus connector on the host board must vary; the "X" and "Y" in Table 3-1 are the high order port addresses for each Multimodule connector as determined by the host iSBC microcomputer board. The port addresses vary according to whether an 8-bit board or a 16-bit board is used as the host iSBC microcomputer board.

3-4. COMMAND EXECUTION SEQUENCE

The Multimodule board is capable of responding to 16 different HDLC/SDLC protocol-related commands for the 8273 device and accepting commands for operation of the 8254 PIT, depending on the I/O port address used in accessing the iSBX 352 board and depending on the type of operation performed (READ or WRITE).

An HDLC/SDLC protocol command is issued to the 8273 device on the iSBX 352 board by filling the required 8273 registers. Once the registers are filled, the 8273 device executes the command, performs any data transfer required, and encodes/decodes the data to/from SDLC/HDLC communications protocol. Each command executed by the 8273 may be subdivided into three phases: a command phase, an execution phase, and a result phase. Each is detailed in the following text.

Table 3-1. I/O Port Addresses

Port Address		Device Selected	Function Performed	
8-Bit	16-Bit			
X0	X0	SELECT 8254 Counter 0	READ WRITE	value from PIT Counter 0. value into Counter 0.
X1	X2	SELECT 8254 Counter 1	READ WRITE	value from PIT Counter 1. value into Counter 1.
X2	X4	SELECT 8254 Counter 2	READ WRITE	value from PIT Counter 2. value into Counter 2.
X3	X6	SELECT 8254 Control	READ WRITE	illegal. value into the PIT Control Register.
X4	X8	SELECT 8273 Command/Status	READ WRITE	Status Register value. Command Register value.
X5	XA	SELECT 8273 Result/Parameter	READ WRITE	Result Register value. Parameter Register value.
X6	XC	SELECT 8273 TxIR/Reset	READ WRITE	Transmit Interrupt Result (TxIR) Register value. RESET.
X7	XE	SELECT 8273 RxIR	READ WRITE	Receive Interrupt Result (TxIR) Register value. illegal.
Y0	Y0	SELECT 8273 Data Receive (RxDACK/)	READ WRITE	RECEIVE data. illegal.
Y4	Y8	SELECT 8273 Data Transmit (TxDACK/)	READ WRITE	illegal. TRANSMIT data.

NOTES:

Refer to the Hardware Reference Manual for your host iSBC microcomputer to determine the upper digit (either X or Y) of the Multimodule port address.

X corresponds with activation of the MCS0/ interface signal; Y corresponds with the activation of the MCS1/ interface signal.

3-5. COMMAND PHASE

During the command phase, the host iSBC microcomputer must execute output instructions that place a command byte into the Command Register and a sequence of command parameters into the Parameter Register within the 8273. The parameter for the Command Register is loaded into the 8273 via port address X4; the remaining parameters are loaded into the Parameter Register via port address X5. The parameters provide for the 8273 a general description of the type of operation that is required.

A command consists of several bytes of information that must all be loaded into the 8273 in a sequence as flowcharted in Figure 3-2. As the flowchart shows, a parameter cannot be sent to the 8273's Command Register when the Command Busy indicator (CBSY at bit 7) in the Status Register is active and a parameter cannot be sent to the 8273's Parameter Register when the Command Parameter Busy bit (CPBF at bit-5) of the Status Register is active.

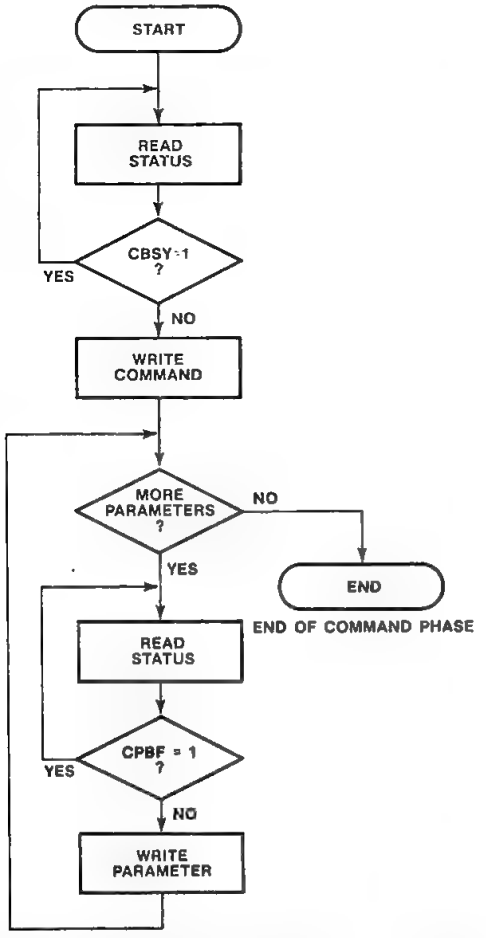


Figure 3-2. Command Phase Flowchart

The commands for the iSBX 352 board are listed in abbreviated form in Table 3-2 and listed in greater detail in the subsequent text.

It is possible to issue commands to cause the iSBX 352 board to operate in both a transmit mode and a receive mode simultaneously (allowed by the design of the 8273). This condition can be initiated by first writing one command and its associated parameters into the 8273 (which initiates one operation) and then writing the second command and its associated parameters immediately following. When performing such an operation, ensure that the status byte from the 8273 is used properly to check the status of the 8273 device on the iSBX 352 board. More information on the operation of the Status Register is contained in paragraph 3-6.

3-6. EXECUTION PHASE

The execution phase begins when the last parameter for the command is loaded into the iSBX 352 board. As the command is loaded into the 8273, the device decodes the type of command and determines how many bytes of parameter are required in the Parameter Register within the 8273. Once the correct number of parameters is received, the 8273 begins execution of the command without further user intervention.

The execution phase of an operation may consist of a data transfer operation or an interrupt driven operation. Intervention of the CPU into the operation is eliminated if a data transfer type command is issued to the iSBX 352 board; that is, the 8273 handles the data request/transfer coordination between the 8273 and the CPU on the host iSBC microcomputer via the TxDRQ and RxDRQ signals, typically used as interrupts to the host. For other data transfer operations, the 8273 generates interrupt request signals (TxINT and RxINT) in the status byte and relies on the CPU on the host to poll the status register to determine the status of the operation.

In buffered transmit mode, the 8273 transmits a Beginning flag automatically, reads the Address and Control registers, transmits the fields, and fetches the Information field via a data transfer operation. After transmitting the Information field, the 8273 automatically appends the Frame Check Sequence character and the Ending flag. Correspondingly, in buffered read mode, the Address and Control fields are stored in their respective buffer registers and only the Information field is transferred to memory.

In non-buffered transmit mode, the 8273 transmits the Beginning flag automatically, then fetches and transmits the Address, Control, and Information

fields from the memory, appends the Frame Check Sequence character and an Ending flag. In the non-buffered receive mode the entire contents of a frame are sent to memory with the exception of the flags and Frame Check Sequence character.

The end of the execution phase is indicated when the contents of the Status Register change. The generation of an interrupt request from the 8273 in an interrupt driven mode of operation indicates via the RxIRA or TxIRA status bits (bits 1 and 2 in the Status Register) that the operation is completed and another command can be issued.

3-7. RESULT PHASE

The execution phase is followed by a result phase in which the host iSBC microcomputer polls one or more of the following registers to determine the outcome of the command execution phase just completed: the Status Register, the Result Register, the RxIR Register, or the TxIR Register (the registers are detailed later in the text). The programming sequence required in the result phase of the operation is shown in Figure 3-3. The result phase can report two types of execution results to the host iSBC

Table 3-2. 8273 Command Summary

Command Description	Command (HEX)	Parameter	Results	Result Port	Completion Interrupt
Set One Bit Delay	A4	Set Mask	None	—	No
Reset One Bit Delay	64	Reset Mask	None	—	No
Set Data Transfer Mode	97	Set Mask	None	—	No
Reset Data Transfer Mode	57	Reset Mask	None	—	No
Set Operating Mode	91	Set Mask	None	—	No
Reset Operating Mode	51	Reset Mask	None	—	No
Set Serial I/O Mode	A0	Set Mask	None	—	No
Reset Serial I/O Mode	60	Reset Mask	None	—	No
General Receive	C0	B0,B1	RIC,R0,R1,A,C*	RxIR	Yes
Selective Receive	C1	B0,B1,A1,A2	RIC,R0,R1,A,C*	RxIR	Yes
Selective Loop Receive	C2	B0,B1,A1,A2	RIC,R0,R1,A,C*	RxIR	Yes
Receive Disable	C5	None	None	—	No
Transmit Frame	C8	L0,L1,A,C#	TIC	TxIR	Yes
Loop Transmit	CA	L0,L1,A,C#	TIC	TxIR	Yes
Transmit Transparent	C9	L0,L1	TIC	TxIR	Yes
Abort Transmit Frame	CC	None	TIC	TxIR	Yes
Abort Loop Transmit	CE	None	TIC	TxIR	Yes
Abort Transmit Transparent	CD	None	TIC	TxIR	Yes
Read Port A	22	None	Port Value	Result	No
Read Port B	23	None	Port Value	Result	No
Set Port B Bit	A3	Set Mask	None	—	No
Reset Port B Bit	63	Reset Mask	None	—	No
Reset Device	01 00				

NOTES:

\# Issued only when in buffered mode.
* Read as results only in buffered mode.

Abbreviations:

B0 — Least significant byte of the receive buffer length.
B1 — Most significant byte of the receive buffer length.
L0 — Least signifiant byte of the Tx frame length.
L1 — Most significant byte of the Tx frame length.
A1 — Receive frame address match field one.
A2 — Receive frame address match field two.
A — Address field of received frame. If non-buffered mode is specified, this result is not provided.
C — Control field of received frame. If non-buffered mode is specified, this result is not provided.
RxIR — Receive Interrupt Result register.
TxIr — Transmit Interrupt Result register.
R0 — Least significant byte of the length of the frame received.
R1 — Most significant byte of the length of the frame received.
RIC — Receiver interrupt result code.
TIC — Transmitter interrupt result code.

microcomputer; either successful completion (no errors detected) or unsuccessful completion (error detected). The results of an operation are made available to the host board in one of two methods (immediate results or non-immediate results), depending on the requirements of the application software.

An immediate result provides an indication of the status of the interface. The immediate result is available to the host iSBC microcomputer from the iSBX 352 board by writing command code 22H to the Command Register in the 8273 (port address X4) and then reading from the Result Register in the 8273 (port address X5) the Port A status (port B status can

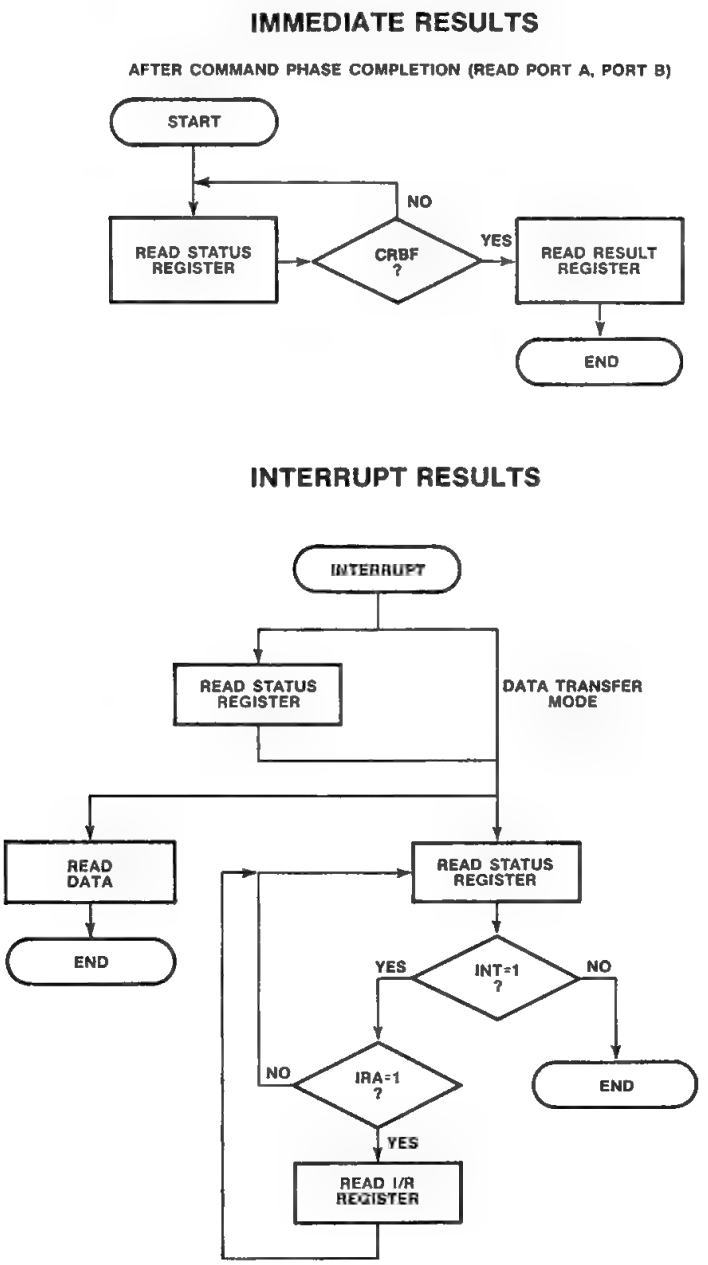


Figure 3-3. Result Phase Flowchart

be read in the same manner using command code 23H). The ports contain information (CTS/, RTS/, etc.) that a network software application can use to make quick operational decisions.

A non-immediate result is generated when the status for an operation is generated with an interrupt signal from the 8273 (either RxINT or TxINT). The non-immediate result is available to the host iSBC microcomputer from the iSBX 352 board by reading either the TxIR Register or the RxIR Register in the 8273 (port addresses X6 and X7, respectively). The registers may contain a one byte interrupt code describing the conditions of the interrupt and, if required, may contain more bytes describing the details of the conditions. The additional bytes are read by issuing successive read commands.

The programming examples in paragraph 3-51 show the sequence required for accessing the contents of the RxIR Register and the TxIR Register.

3-8. COMMAND DESCRIPTION

The 8273 Programmable HDLC/SDLC Protocol Controller supports a comprehensive set of high level commands which allows the 8273 to be readily used in full-duplex, half-duplex, synchronous, asynchronous, point-to-point, and loop configurations. The commands minimize CPU and software overhead. The 8273 contains byte-wide address and control buffers which allow the receive and transmit commands to be used in buffered or non-buffered modes.

There are six basic types of commands available for use with the 8273; the initialization set/reset commands, the reset device command, the receive commands, the transmit commands, the abort transmit commands, and the modem control commands. Table 3-2 contains a brief description of each command including the number of parameters required for execution of each. A detailed description of the commands is contained in the following paragraphs.

3-9. INITIALIZATION SET/RESET COMMANDS

The 8273 supports the use of eight initialization set/reset commands as follows: Set One Bit Delay, Reset One Bit Delay, Set Data Transfer Mode, Reset Data Transfer Mode, Set Operating Mode, Reset Operating Mode, Set Serial I/O Mode, and Reset Serial I/O Mode. These eight commands are used in manipulating the registers internal to the 8273 that define the various operating modes. One parameter is required for each command.

The set commands require a mask parameter that performs a logical-OR of the specified 8273 register with the mask bits provided as a parameter. The reset commands require a mask parameter that performs a logical-AND of the contents of the specified register and the mask. Each of the eight commands is described in greater detail in the following paragraphs.

3-10. SET ONE-BIT DELAY (Command Code A4)

When the Set One-Bit Delay command is issued to the iSBX 352 board, the 8273 retransmits the received data stream one bit delayed. This mode is entered and exited at a receiver character boundary, and should only be used by loop stations. When reset, the receive and transmit data are independent.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command A4:	1	0	1	0	0	1	0	0
Parameter 80:	1	0	0	0	0	0	0	0

3-11. RESET ONE-BIT DELAY (Command Code 64)

When the Reset One-Bit Delay command is issued to the iSBX 352 board, the 8273 leaves the one-bit delayed retransmission mode of operation. The data transmitted may not be the same data that was received. On detection of the command, the 8273 device enters an idle mode until another mode is selected.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command 64:	0	1	1	0	0	1	0	0
Parameter 7F:	0	1	1	1	1	1	1	1

3-12. SET DATA TRANSFER MODE (Command Code 97)

When the Set Data Transfer Mode command is sensed and parameter bit 0 is set, the 8273 will interrupt the host iSBC microcomputer when data bytes are required for transmit operation or when data bytes are available from a receive operation. If a transmit interrupt occurs and the Status register contents indicate that there is no Transmit Result (TxIRA = 0), the interrupt is considered to be a transmit data request. If a receive interrupt occurs and the status indicates that there is no receive result (RxIRA = 0), the interrupt is considered to be a receive data request. When the Set Data Transfer Mode command is sensed and parameter bit 0 is reset, the 8273 generates data transfer requests on the DRQ lines

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command 97:	1	0	0	1	0	1	1	1
Parameter 01:	0	0	0	0	0	0	0	1

3-13. RESET DATA TRANSFER MODE (Command Code 57)

The Reset Data Transfer Mode command allows resetting of the data transfer mode in the 8273. If the Data Transfer Mode is reset, the data transfer requests are handled via TxDRQ and RxDRQ rather than TxINT and RxINT.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command 57:	0	1	0	1	0	1	1	1
Parameter FE:	1	1	1	1	1	1	1	0

3-14. SET OPERATING MODE (Command Code 91)

The Set Operating Mode command allows a user to select the following operating modes:

Flag Stream Mode
Preframe Sync Mode
Buffered Mode
Early Interrupt Mode
EOP Interrupt Mode
HDLC Mode.

Each is described in the following paragraphs.

(D5) HDLC Mode

When the bit is set, a bit sequence of seven ones (01111111) is interpreted as an abort character and generates an interrupt. When the bit is reset, a bit sequence of eight ones (011111111) is interpreted as an abort character and generates an interrupt.

(D4) EOP Interrupt Mode

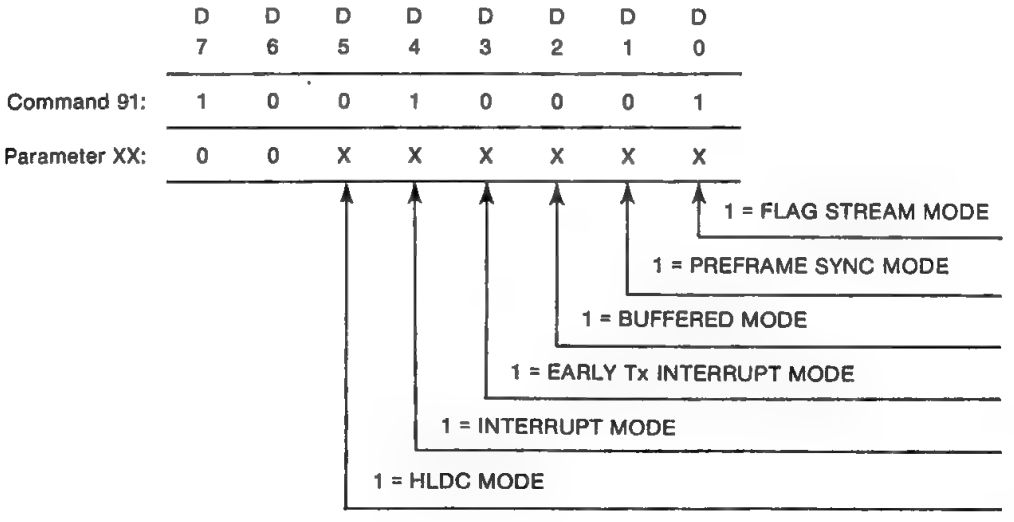
When the bit is set, an interrupt is generated whenever an EOP character (01111111) is detected by an active receiver. This mode is useful for the implementation of an SDLC loop controller in detecting the end of a message stream after a loop poll. No EOP interrupt is generated at the end of a loop transmission when this bit is reset.

(D3) Transmitter Early Interrupt Mode (Tx)

The Transmitter Early Interrupt Mode indicates when the 8273 should generate an end of frame interrupt. When the Transmitter Early Interrupt bit is set, an interrupt is generated as the last data character is passed to the 8273. If the user software responds with another transmit command within two byte times, the final flag interrupt will not be generated and a new frame will immediately begin when the current frame is complete; this permits frames to be separated by a single flag. If the delay is more than two byte times, then more than one flag separates the frames and a frame completed interrupt is generated. If this bit is zero, the interrupt will be generated only after the final flag has been transmitted. If transmitting a supervisory frame in buffered mode, refer to the *Intel 1981 Data Catalog* for more information.

(D2) Buffered Mode

If the Buffered Mode bit is set to a one, the first two bytes (normally the Address (A) and Control (C) fields) of received frames are buffered by the 8273 and passed to the host iSBC microcomputer as results after a Received Frame interrupt. On transmit, the Address and Control fields are passed to the 8273 as parameters. If this bit is a zero, the Address and Control fields are passed to and from memory.



(D1) Preframe Sync Mode

If this bit is set, the 8273 will transmit two characters before the Begining flag of a frame. These characters provide 16 line transitions to ensure synchronization of the opposing receiver. To guarantee sixteen line transitions, the 8273 sends two bytes of data; either 00H-00H if NRZI is selected or 55H-55H if NRZI is not selected. If the bit is reset, no preframe sync characters are sent.

(D0) Flag Stream Mode

If this bit is set, the transmitter begins sending flag characters as soon as it goes inactive. Table 3-3 defines the operation of the transmitter when the bit is set. If this bit is reset, the transmitter begins sending idle characters as soon as it goes inactive. Table 3-4 outlines the operation of the transmitter when the bit is reset.

Table 3-3. Transmitter Operating Modes — Flag Stream Mode

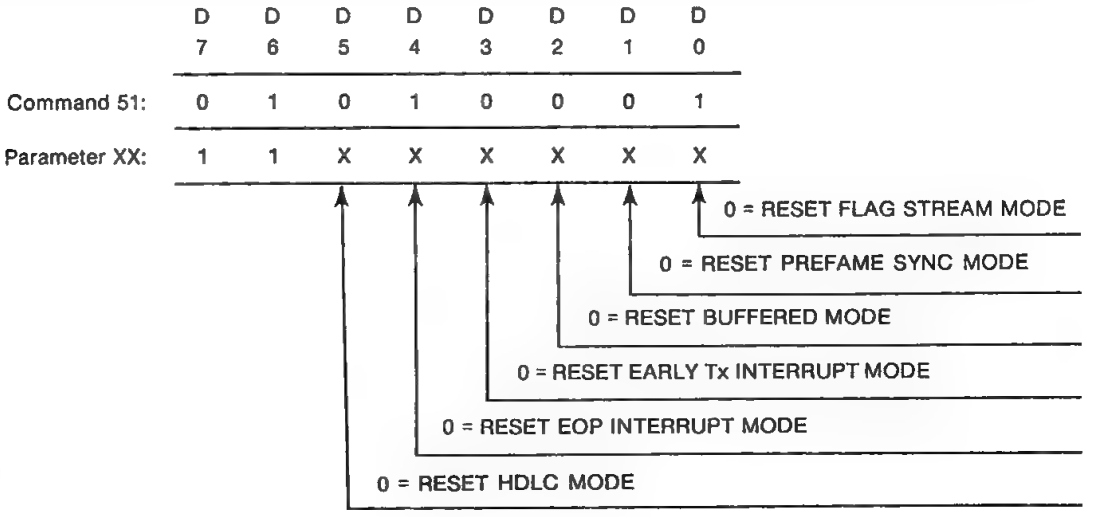
TRANSMITTER STATE	ACTION
Idle	Send flag characters immediately.
Transmit or Transmit-Transparent Active	Send flag characters after the transmission is complete.
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.

Table 3-4. Transmitter Operating Modes — Non Flag Stream Mode

TRANSMITTER STATE	ACTION
Idle	Send idle characters on next character boundary.
Transmit or Transmit-Transparent Active	Send idle characters after the transmission is complete.
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.

3-15. RESET OPERATING MODE (Command Code 51)

The Reset Operating Mode command allows any mode switches set via Command Code 91 (Set Operating Mode) to be reset using this command by placing zeros in the appropriate mask bit positions.



3-16. SET SERIAL I/O MODE (Command Code A0)

The Set Serial I/O Mode command, when issued to an iSBX 352 board, allows configuation of the serial I/O port's operating mode by placing ones into the appropriate bit positions of a mask byte.

(D2) Loopback Data

If this bit is set, the transmitted data (TxD) is internally routed to the receive data (RxD) circuitry. When reset, the bit allows TxD and RxD to remain independent of each other.

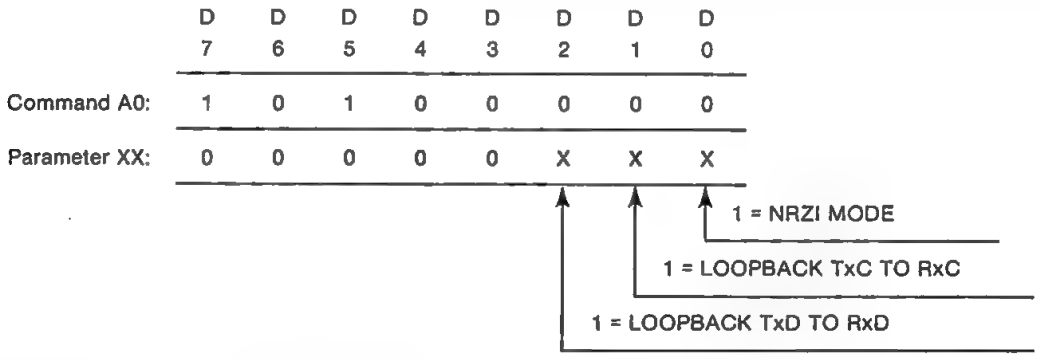
(D1) Loopback Clock

If this bit is set, the transmit clock (TxC) is internally routed to the receive clock (RxC) circuitry; normal use is with the loop back bit (D2). If the bit is reset, the clocks remain independent.

(D0) NRZI Mode

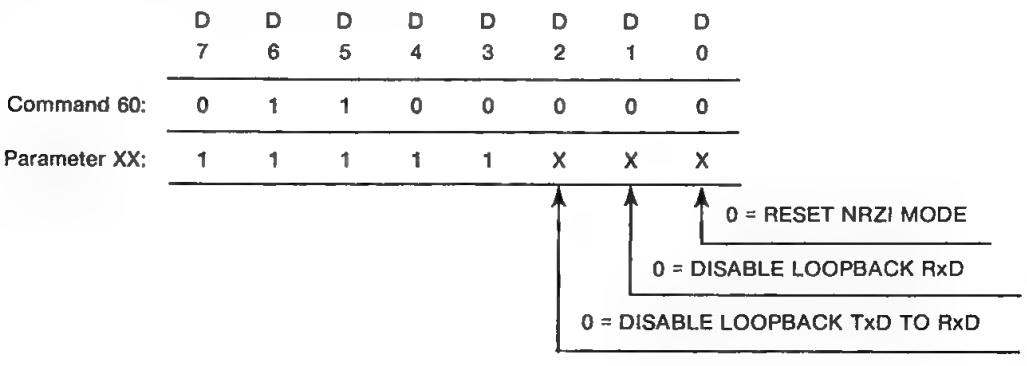
If this bit is set, the 8273 assumes that the receive data is NRZI encoded and procedes to encode the transmit data. If this bit is reset, the transmit and receive data are treated as a normal positive logic bit stream.

NRZI encoding specifies that a zero causes a change in the polarity of the transmitted signal and a one causes no polarity change. NRZI is used in all asynchronous operations. Refer to the *IBM Synchronous Data Link Control, General Information Manual* for details.



3-17. RESET SERIAL I/O MODE (Command Code 60)

The Reset Serial I/O Mode command allows bits set in Command Code A0 (Set Serial I/O Mode) to be reset by placing zeroes in the appropriate mask positions.



3-18. RESET DEVICE COMMAND

The iSBX 352 board supports one program controlled reset command. The Reset Device command is issued to the 8273 on the iSBX 352 board by outputting 01H followed by 00H to the Reset Mode Register. Since the 8273 requires time to process the reset signal internally, at least 2.5 microseconds should separate the writing of the 01H parameter and the writing of the 00H parameter to the Test Mode Register. The program controlled reset emulates the action of the hardware reset, as follows:

1. The modem control signals are forced high (inactive level).
2. The 8273 Status register is cleared.
3. Any commands in progress are terminated immediately.
4. The 8273 enters an idle state until the next command is issued.
5. The iSBX 352 board assumes a non-loop SDLC terminal role.

Refer to the programming examples for an example of the coding required for the operation.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
TMR:	0	0	0	0	0	0	0	1
TMR:	0	0	0	0	0	0	0	0

3-19. RECEIVE COMMANDS

The iSBX 352 board supports three types of receive commands: General Receive, Selective Receive, and Selective Loop Receive. Each is issued to the 8273 device and described in the following paragraphs.

3-20. GENERAL RECEIVE (Command Code C0)

When commanded to General Receive, the 8273 passes all frames to the host iSBC microcomputer regardless of the contents of the Address field within the frame. The General Receive command is used primarily for loop controlling stations. Two parameters are required: B0 and B1, as shown. The parameters provide the buffer size to the 8273 and allow it to monitor for buffer overflow. The 8273 generates an interrupt to the host iSBC microcomputer if the received frame attempts to overfill the specified buffer space.

When a frame is received without error, the 8273 interrupts the host iSBC microcomputer following the Ending flag. On receiving an interrupt, the host must then read up to 4 bytes of results of the operation from the RxIR Register. If operating in the Buffered Mode, the 8273 contains the Receiver Interrupt Result code, the byte length of the Information field received in the frame (two bytes listed as R0 and R1) low byte first, the contents of the Address field, and the contents of the Control field in the RxIR Register. If operating in the Non-Buffered Mode, the 8273 contains only the Receiver Interrupt Result code and the byte length of the Information field received in the frame (two bytes listed as R0 and R1) low byte first; the Address and Control field parameters are ignored by the RxIR Register.

NOTES:

1. If buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received.
2. If non-buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received plus two (the count includes the address and control bytes).
3. The frame check sequence (FCS) is not transferred to memory.
4. Frames with less than 32 bits between flags are ignored (no interrupt generated) if the buffered mode is specified.
5. In the non-buffered mode an interrupt is generated when a less than 32 bit frame is received, since data transfer requests have occurred.

6. The 8273 receiver is always disabled when an Idle is received after a valid frame. The CPU module must issue a receive command to re-enable the receiver.
7. The intervening ABORT character between a final flag and an IDLE does not generate an interrupt.
8. If an ABORT Character is not preceded by a flag and is followed by an IDLE, an interrupt will be generated for the ABORT followed by an IDLE Interrupt one character time later. The reception of an ABORT will disable the receiver.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	0	0	0	0
Parameter:	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)							
Parameter:	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)							

3-21. SELECTIVE RECEIVE (Command Code C1)

The Selective Receive command requires two additional parameters: A0 and A1, the address match bytes. When the Selective Receive command is issued to the iSBX 352 board, the 8273 device is placed into a receive mode in which frames are ignored unless the Address field matches any one of two address match bytes given to the 8273 as parameters. When the Selective Receive command is issued, the 8273 passes to the host iSBC microcomputer only those frames containing an Address field that matches either A0 or A1. The command is usually used with secondary stations with A1 being the secondary's parameter and A2 being the "all parties" parameter. If only one byte is needed, set A1 and A2 equal. As in the General Receive command, the 8273 counts the number of incoming data bytes and interrupts if the byte count (B0 and B1) is exceeded.

When a frame is received without error, the 8273 interrupts the host iSBC microcomputer following the Ending flag. On receiving an interrupt, the host must then read up to 4 bytes of results of the operation from the RxIR Register. If operating in the Buffered Mode, the 8273 contains the Receiver Interrupt Result code, the byte length of the Information field received in the frame (two bytes listed as R0 and R1) low byte first, the contents of the Address field, and the contents of the Control field in the RxIR Register. If operating in the Non-Buffered Mode, the 8273 contains only the Receiver Interrupt Result code and the byte length of the Information field received in the frame (two bytes listed as R0 and R1) low byte first; the Address and Control field parameters are ignored by the RxIR Register.

NOTE

The iSBX 352 board cannot perform a Selective Loop Receive when generating HDLC protocol; an abort character (8 ones) is decoded the same as an EOP character (7 ones).

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	0	0	0	1
Parameter:	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)							
Parameter:	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)							
Parameter:	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)							
Parameter:	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)							

3-22. SELECTIVE LOOP RECEIVE (Command Code C2)

Selective Loop Receive command operates like the Selective Receive command except that One-Bit Delay Mode must be set and, following a received frame, the 8273 holds the loop active by placing its transmitter into Flag Stream Mode automatically after detection of an EOP character (01111111).

NOTE

When a frame is received without error, the 8273 interrupts the host iSBC microcomputer following the Ending flag. On receiving an interrupt, the host must then read up to 4 bytes of results of the operation from the RxIR Register. If operating in the Buffered Mode, the 8273 contains the Receiver Interrupt Result code, the byte length of the Information field received in the frame (two bytes listed as R0 and R1) low byte first, the contents of the Address field, and the contents of the Control field in the RxIR Register. If operating in the Non-Buffered Mode, the 8273 contains only the Receiver Interrupt Result code and the byte length of the Information field received in the frame (two bytes listed as R0 and R1) low byte first; the Address and Control field parameters are ignored by the RxIR Register.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	0	0	1	0
Parameter:	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)							
Parameter:	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)							
Parameter:	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)							
Parameter:	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)							

3-23. RECEIVER DISABLE (Command Code C5)

The Receive Disable command terminates an active receive command immediately. No parameters are required and no results are generated for the operation in the RxIR Register. The 8273 enters an idle mode on detection of a Receiver Disable command.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	0	1	0	1
Parameter:	NONE							

3-24. TRANSMIT COMMANDS

The 8273 supports three transmit commands: Transmit Frame, Loop Transmit, and Transmit Transparent. Each is described individually in the following paragraphs.

3-25. TRANSMIT FRAME (Command Code C8)

The Transmit Frame command, when issued to the iSBX 352 board, causes the 8273 device to transmit one frame including the Beginning flag, Frame Check Sequence character, and the Ending flag. Four parameters are required when the 8273 operates in Buffered Mode; two when in Non-Buffered Mode.

In Buffered Mode 8273 operation, the first two parameters must be the least and most significant bytes of the desired frame length (L0 and L1). The frame length specifies the length in bytes of the desired Information field. The Address and Control fields are passed to the transmitter as the third and fourth parameters, respectively.

In Non-Buffered Mode 8273 operation, the frame length parameter provided as L0 and L1 must consist of the length of the Information field plus two (specifying the number of data transfers to be performed). The Address and Control fields must be passed to the transmitter as the first two bytes of data.

The Transmit Frame command causes the 8273 to activate the RTS signal and then wait for activation of the CTS signal. On receiving CTS, the 8273 begins transferring a frame. On completion of the transfer, the 8273 generates an interrupt to the host iSBC microcomputer and then enters either an Idle mode or a Flag Stream mode. If the RTS signal was active before the operation, the 8273 does not change it. If the RTS signal was inactive, the 8273 deactivates it within one character time.

On receiving the interrupt, the host iSBC microcomputer may retrieve transmit status for the transmit operation from the iSBX 352 board by reading the contents of the TxIR Register in the 8273.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	1	0	0	0
Parameter:	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
Parameter:	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							
Parameter:	ADDRESS FIELD OF TRANSMIT FRAME (A)							
Parameter:	CONTROL FIELD OF TRANSMIT FRAME (C)							

3-26. LOOP TRANSMIT (Command Code CA)

The Loop Transmit command, when issued to the iSBX 352 board, allows the 8273 device to transmit one frame in the same manner as the Transmit Frame command except:

1. If the flag stream mode is not active, transmission will begin after a received EOP has been converted to a flag.
2. If the flag stream mode is active, transmission will begin at the next flag boundary for buffered mode or at the third flag boundary for non-buffered mode.
3. At the end of a loop transmit the one-bit delay mode is entered and the flag stream mode is reset.

The parameter definitions for the Loop Transmit command are the same as for the Transmit Frame command. Since the command deals with loop configurations, the 8273 device must be operating in One-Bit Delayed Mode (refer to the One-Bit Delay Command description).

If the transmitter is not in Flag Stream Mode (see Set Operating Mode command) when Loop Transmit command is received, the transmitter waits until after a received EOP character is converted to a flag (done automatically by the 8273) before transmitting. If the transmitter is already in Flag Stream Mode as a result of

a Selective Loop Receive command, frame transmission begins at the next flag boundary if in Buffered Mode (at the third flag boundary if in Non-Buffered Mode). The extra frames in non-Buffered Mode fill the internal transmit buffer in the 8273. At the end of a Loop Transmit command, the 8273 enters the One-Bit Delay Mode and resets the Flag Stream Mode.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	1	0	1	0
Parameter:	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
Parameter:	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							
Parameter:	ADDRESS FIELD OF TRANSMIT FRAME (A)							
Parameter:	CONTROL FIELD OF TRANSMIT FRAME (C)							

3-27. TRANSMIT TRANSPARENT (Command Code C9)

When issued a Transmit Transparent command, the iSBX 352 board enables the 8273 to transmit a block of raw data without HDLC/SDLC protocol; i.e., no zero bit insertion, no Beginning flag, no Ending flag, no Address field, no Control field, and no Frame Check Sequence characters are added during the transfer. Only the L0 and L1 parameters are required since there is no Address field or Control field for this command. The command makes it possible to construct and transmit a BISYNC protocol message and may be useful in performing diagnostic routines on the iSBX 352 boards.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	1	0	0	1
Parameter:	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
Parameter:	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							

3-28. ABORT TRANSMIT COMMANDS

An abort command is supported for each type of transmit command. The abort commands are ignored if a transmit command is not in progress. The abort commands require no parameters and provide a status indication in the TxIR Register for the host iSBC microcomputer.

3-29. ABORT TRANSMIT FRAME (Command Code CC)

When the Abort Transmit command is issued to the iSBX 352 board, the 8273 begins searching for an Ending flag. Once the flag is found, the 8273 sends the abort character. After an abort character (eight contiguous ones) is transmitted, the transmitter reverts to sending flags or idles as a function of the Flag Stream Mode specified (refer to Set Operating Mode command).

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	1	1	0	0
Parameter:	NONE							

3-30. ABORT LOOP TRANSMIT (Command Code CE)

The Abort Loop Transmit command, when issued properly to the iSBX 352 board, allows the transmitter within the 8273 to revert to one bit delay mode operation after a Beginning or Ending flag is transmitted.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	1	1	1	0
Parameter:	NONE							

3-31. ABORT TRANSMIT TRANSPARENT (Command Code CD)

When an Abort Transmit Transparent command is issued to the iSBX 352 board, the command allows the transmitter within the 8273 to revert to sending flags or idles on detection of the next flag. The operation is a function of the Flag Stream Mode specified.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	1	0	0	1	1	0	1
Parameter:	NONE							

3-32. MODEM CONTROL COMMANDS

The iSBX 352 board supports four basic modem control commands to allow manipulation of the modem control ports. The commands are as follows; Read Port A, Read Port B, Set Port B, and Reset Port B. When the Read Port A or the Read Port B commands are issued to the iSBX 352 board, the 8273 places the condition of the ports into the Result register within the 8273. The Set and Reset Port B Bit commands require a parameter that masks the bits to be set or reset. More details on the operation of each command can be found in the following paragraphs.

3-33. READ PORT A (Command Code 22)

When a Read Port A command is issued to the iSBX 352 board, the command places the data from Port A of the 8273 device into the Result register in the 8273.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	0	0	1	0	0	0	1	0
Result:	1	1	1	X	X	DSR	X	CTS

3-34. READ PORT B (Command Code 23)

The Read Port B command places the data from PB0 through PB7 of Port B into the Result register in the 8273.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	0	0	1	0	0	0	1	1
Result:	1	1	X	X	X	DTR	X	RTS

3-35. SET PORT B BITS (Command Code A3)

The Set Port B command allows the Port B pins to be set as required for the application.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Command:	1	0	1	0	0	0	1	1
Parameter:	0	0	0	X	X	X	X	X

RTS-REQUEST TO SEND

USER DEFINED

(D_2) Data Terminal Ready

This bit provides control over a dedicated 8273 modem control signal, the Data Terminal Ready (DTR) signal, and reflects the logical state of the RTS signal, PB_2 of Port B, on completion of an operation.

(D_0) Request to Send

This bit provides control over a dedicated 8273 modem control signal, the Request To Send (RTS) signal, and reflects the logical state of the RTS signal, PB_0 of Port B, on completion of an operation.

3-36. RESET PORT B BITS (Command Code 63)

The Reset Port B Bits command, when issued to the iSBX 352 board, allows the user-defined bits (PB_4-PB_1) of Port B of the 8273 to be reset when a 0 is placed into the respective mask position. Port B bits 1 through 4 (PB_1-PB_4) correspond to D1 through D4.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Out Command:	0	1	1	0	0	0	1	1
Out Parameter:	1	1	0	X	X	X	X	X

RTS-REQUEST TO SEND

USER DEFINED

3-37. STATUS WORD FORMATS

The status for an operation on the iSBX 352 board consists of the status that is made available from the 8273 device after command execution. The status is contained within several different registers within the 8273 device. The RxIR Register contains up to 5 bytes describing the status of a previous 8273 receive operation plus additional details on the reason for generation of the interrupt. The TxIR Register contains 1 byte describing the status of a previous 8273 transmit operation. When read, the Result Register in the 8273 device provides an immediate result describing the outcome of an executed command. The Status Regiter within the 8273 device provides a 1-byte description of the state of the 8273's interface to the host iSBC microcomputer. Each of the registers previously mentioned provides status information that is required in some situations.

Some commands, such as Read Port A or Read Port B, provide an immediate result. The status for the operation can be obtained by reading the contents of the Status Register and the Result Register in the 8273. Commands that do not provide an immediate result are designed to provide status for the operation when the interrupt is generated. The non-immediate status is available in either the Receive Interrupt Result (RxIR) Register or the Transmit Interrupt Result (TxIR) Register within the 8273 device. The status may consist of a one byte interrupt code indicating the general conditions of the interrupt and perhaps one or more bytes detailing the specific conditions. The four registers are described in the following paragraphs.

3-38. STATUS REGISTER FORMAT (Internal to 8273)

The format of the Status register within the 8273 device is shown in Figure 3-4. The function of each bit of the register is as follows.

CBSY-Command Busy (Bit 7). The CBSY bit of the Status Register indicates that a command execution is in progress. The bit is set whenever a command is present in the internal Command Register within the 8273. The bit is reset by the 8273 when the command phase of an operation is completed. Do not write a command into the 8273 when the CBSY bit is active; the result is an incorrect operation.

CBF-Command Buffer Full (Bit 6). The CBF bit of the Status Register indicates that the Command Register internal to the 8273 device contains a command. The bit is reset when a 8273 accepts a command byte. The bit does not reflect the state of the execution of the command.

CPBF-Command Parameter Buffer Full (Bit 5). The CPBF bit of the Status Register indicates when all command Parameter Register bytes (if more than one is required) are received within the 8273 device. The bit is reset whenever the 8273 accepts a parameter into the Parameter Register.

CRBF-Command Result Buffer Full (Bit 4). The CRBF bit of the Status Regsiter inducates that the immediate result of an executed command is available in the Result Register within the 8273 device. The bit is set by the 8273 on the completion of a command and reset by reading the contents of the Status Register.

RxINT-Receiver Interrupt (Bit 3). The RxINT bit of the Status Register indicates that the receiver portion of the 8273 requires service from the host iSBC microcomputer. The bit is set by the 8273 upon completion of a specified command (either good results or bad). The bit is reset by the host iSBC microcomputer after it reads the Result Register contents. During a data transfer, the bit is reset after the host iSBC microcomputer reads a receive data byte from the 8273.

TxINT-Transmitter Interrupt (Bit 2). The TxINT bit of the Status Register indicates that the transmitter portion of the 8273 requires service from the host iSBC microcomputer. The bit is set by the 8273 upon completion of a specified command (either good results or bad) or during execution of a data transfer. After completing a command, the bit is reset by the host iSBC microcomputer after it reads the Result Register contents. During a data transfer, the bit is reset after the host iSBC microcomputer writes a transmit data byte to the 8273.

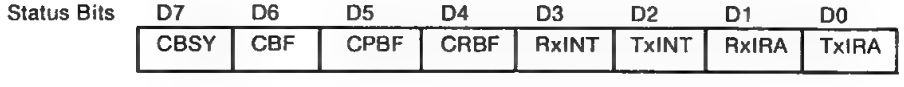


Figure 3-4. Status Register Format

RxIRA-Receiver Interrupt Result Available (Bit 1). The RxIRA bit in the RxIR Register is set by the 8273 when a receiver interrupt result byte is available within the 8273. The bit is reset by after the host iSBC microcomputer reads the register.

TxIRA-Transmitter Interrupt Result Available (Bit 0). The TxIRA bit in the TxIR Register is set by the 8273 when a transmitter interrupt result byte is available within the 8273. The bit is reset by after the host iSBC microcomputer reads the register.

3-39. TRANSMIT INTERRUPT RESULT (TxIR) REGISTER

The Transmit Interrupt Result Byte is a byte of status information collated by the 8273 during a transmit operation and made available to the host iSBC microcomputer when it reads port address X6H (where X is the most significant digit of the Multimodule connector port address as determined on the host iSBC microcomputer). The byte contains status information on a transmit operation as listed in Figure 3-5.

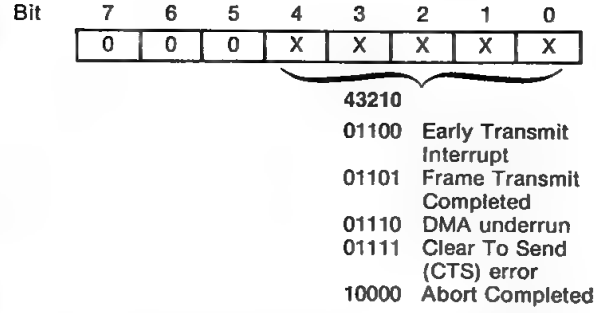


Figure 3-5. Format of Transmit Interrupt Result Codes (TIC) Within Transmit Interrupt Result (TxIR) Register

A transmit operation returns 1 byte of status information, called the Transmit Interrupt Result Code (TIC), in the TxIR Register. Table 3-5 lists the transmit commands that return the TIC.

3-40. RECEIVE INTERRUPT RESULT (RxIR) REGISTER

The Receive Interrupt Result Register contains up to 4 bytes of status information collated by the 8273 during a receive operation and made available to the host iSBC microcomputer when it reads port address X7H (where X is the most significant digit of the Multimodule connector port address as determined on the host iSBC microcomputer). The byte contains status information on a receive operation as listed in Figure 3-6.

Table 3-5. Status for Transmit Commands

Command	Hex Code	Status in TxIR Register after Interrupt
Transmit Frame	C8	TIC
Abort Transmit Frame	CC	TIC
Loop Transmit	CA	TIC
Abort Loop Transparent	CO	TIC
Abort Transmit Transparent	CD	TIC

NOTES:
1. TIC — Transmitter Interrupt Code byte
2. All commands also provide an additional status byte in the Status Register.

Bits 76543210	Receiver Interrupt Type	Receiver Status On Generating Interrupt
Bit 765		
000	Bit 0 received	
001	Bits 0 and 1 received	
010	Bits 0 through 2 received	
011	Bits 0 through 3 received	
100	Bits 0 through 4 received	
101	Bits 0 through 5 received	
110	Bits 0 through 6 received	
111	Bits 0 through 7 received	
***00000	A1 Match or General Receive	Active
***00001	A2 Match	Active
00000011	CRC Error detected	Active
00000100	Abort Character Detected	Active
00000101	Idle Character Detected	Disabled
00000110	EOP Character Detected	Disabled
00000111	Frame Length Less Than 32-bits	Active
00001000	DMA Transfer Overrun Detected	Disabled
00001001	Memory Buffer Overflow	Disabled
00001010	Carrier Detect Failure	Disabled
00001011	Receiver Interrupt Overrun	Disabled

NOTE:
The * indicates the number of bits that are received in the operation.

Figure 3-6. Format of Receiver Interrupt Result Code (RIC) Within Receiver Interrupt Result (RxIR) Register

A receive operation returns up to 5 bytes of status information in the RxIR Register that must be read on successive READ commands directed to the RxIR Register in the 8273 device. Table 3-5A shows the sequence of status bytes returned from the RxIR Register for each type of receive command.

Table 3-5A. Status For Red Commands

Command	Hex Code	Status In RxIR Register after Interrupt
General Receive	C0	RIC, R0, R1, A, C,
Selective Receive	C1	RIC, R0, R1, A, C
Selective Loop Receive	C2	RIC, R0, R1, A, C,
Disable Receiver	C3	no status

NOTES:

1. RIC — Receiver Interrupt Code byte
   R0 — Frame length, least significant byte
   R1 — Frame length, most significant byte
   A — Address field byte within the frame
   C — Control field byte within the frame
2. A and C fields are returned only when 8273 operates in Buffered Mode.
3. All commands also provide an additional status byte in the Status Register.

3-41. 8254 PIT PROGRAMMING

A 24.00 MHz crystal oscillator supplies the basic 8 MHz clock frequency for the PIT. This clock frequency is available for input to the 8254 PIT.

Counter 2 is the only counter in the 8254 PIT that is user configurable. Counter 0 is dedicated to generation of the TxC Clock for the 8273 device and Counter 1 is dedicated to generation of the 32-times Clock required as a data transfer clock for the 8273 device. Counter 1 can be used as a general purpose timer when the iSBX 352 board is operating in a synchronous mode.

The outputs of Counter 0 and Counter 1 are dedicated, so ensure that both counters are programmed properly. When programming Counter 2 of the 8254 PIT, ascertain the clock output functions that are required.

3-42. MODE CONTROL WORD AND COUNT

All three counters must be initialized via user programming prior to their use. The initialization for each counter consists of two steps:

a. A mode control word (Figure 3-7) is written to the Control register for each individual counter.

b. A count number is loaded into each counter. The count number is in one or two 8-bit bytes as determined by the mode control word.

The mode control word (Figure 3-7) does the following:

a. Selects the counter to be loaded.

b. Selects operating mode of the counter.

c. Selects one of the following four counter read/load functions:
   (1) Counter latch (for stable read operation).
   (2) Read or load most-significant byte only.
   (3) Read or load least-significant byte only.
   (4) Read or load least-significant byte first, followed by most-significant byte.

d. Sets the counter for either binary or BCD count operation.

The mode control word and the count register bytes for any given counter must be entered in the following sequence:

a. Mode control word.

b. Least-significant count register byte (if required).

c. Most-significant count register byte (if required).

As long as the procedure is followed, each counter in the chip can be programmed in any convenient sequence. For example, mode control words can be loaded into Counter 0, followed by the least-significant byte, most-significant byte, etc and then Counter 1 can be loaded followed by Counter 2. The counters can be loaded in any order so long as the correct number of bytes is loaded into each counter in order. Figure 3-8 shows the programming sequence described previously.

Since the counters in the PIT chip are down counters, the value loaded into each counter is decremented. Loading all zeros into the count register results in a maximum count of 2^{16} for binary numbers or 10^4 for BCD numbers.

The count mode selected in the control word controls the counter output. As mentioned earlier, Counter 0 and Counter 1 on the iSBX 352 board are dedicated to providing clocks for the 8273 device, the counters must be initialized in the square wave generator mode of operation (Mode 3). Counter 2 can be programmed to operate in any desired mode. As shown in Figure 3-7, Counter 2 in the PIT can operate in four of six possible modes, as follows:

a. Mode 0: Interrupt on terminal count. In this mode, the counters can be used for auxillary functions, such as generating real-time interrupt intervals. After the count value is loaded into the count register, the counter output goes low and remains low until the terminal count is reached. The output then goes high until the count register is reloaded or the mode is reloaded.

b. Mode 1: Programmable one-shot. This mode of operation is not available on the iSBX 352 board.

c. Mode 2: Rate generator. In this mode, the output of the counters will be low for one period of the clock input. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected but the subsequent period will reflect the new value. When mode 2 is set, the output will remain high until after the count register is loaded; thus, the count can be synchronized by software.

d. Mode 3: Square wave generator. In this mode, the counter output remains high until one-half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (N + 1)/2 counts,and low for (N -1)/2 counts.

e. Mode 4: Software triggered strobe. After this mode is set, the output will be high. When the count is loaded, the counter begins counting. On terminal count, the output will go low for one input clock period and then go high again. If the count register is reloaded between output pulses, the present count will not be affected, but the subsequent period will reflect the new value. Reloading the count register will restart the counting for the new value.

f. Mode 5: Hardware triggered strobe. This mode of operation is not supported on the iSBX 352 board.

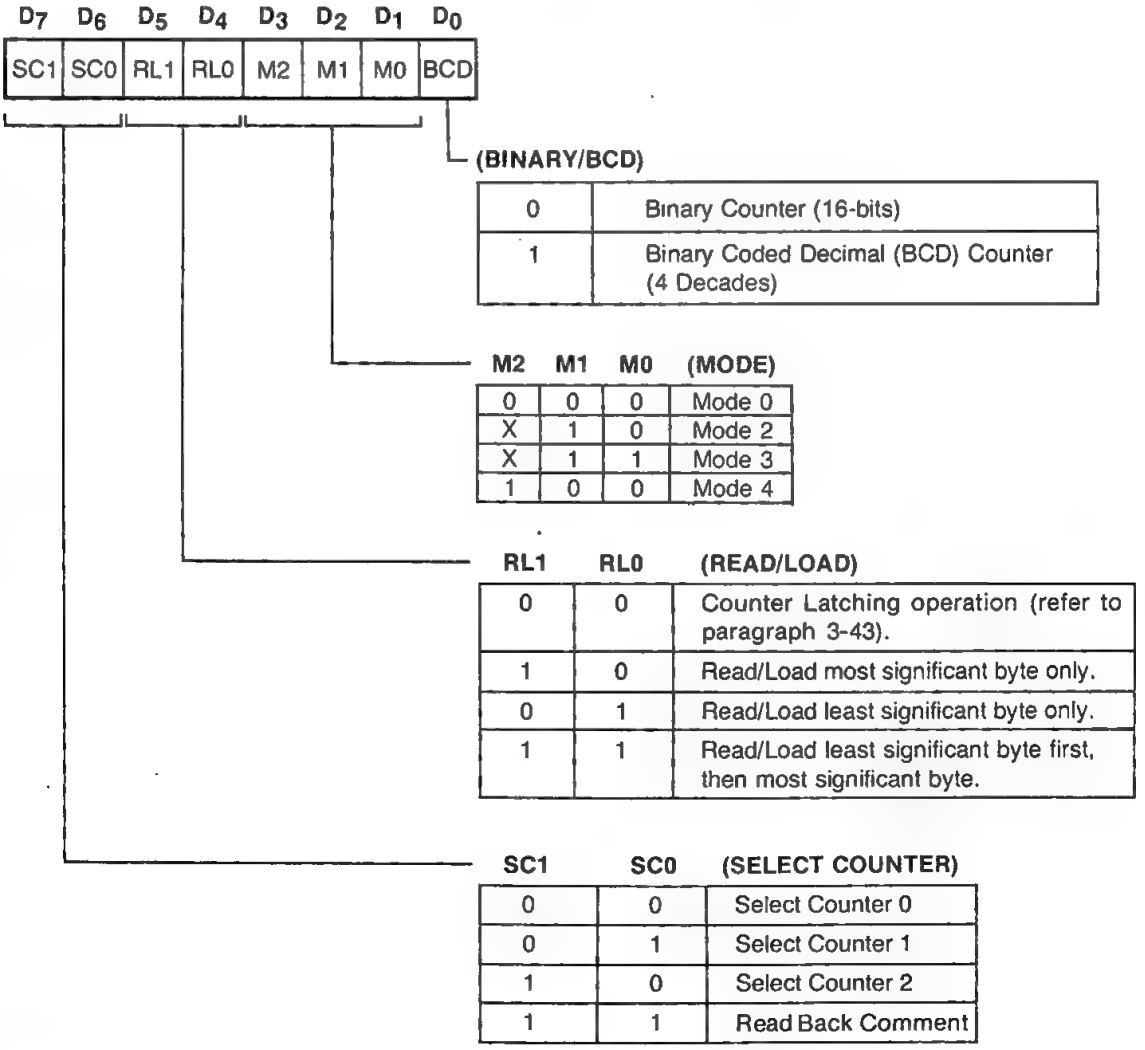


Figure 3-7. PIT Control Word Format

PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

Figure 3-8. PIT Programming Sequence Examples

3-43. ADDRESSING

As listed in Table 3-1, the PIT uses four I/O port addresses. I/O port addresses base+0, base+1, and base+2, respectively, are used in loading and reading the count in Counters 0, 1, and 2. I/O port address base+3 is used in writing the mode control word to the desired counter. Refer to Table 3-1 for more port addressing information.

3-44. INITIALIZATION

To initialize the PIT chip, perform the following:

a. Write a mode control word for Counter 0 to I/O port address base+3. Note that all mode control words are written to base+3, since the mode control word must specify which counter is being programmed. (Refer to Figure 3-7.)

   Table 3-6 provides a sample subroutine for writing mode control words to all three counters.

b. Assuming the mode control word has selected a 2-byte load, load least-significant byte of count into Counter 0 at I/O port address base+0. (Count value to be loaded is described in paragraph 3-44.) Table 3-7 provides a sample subroutine for loading a 2-byte count value.

c. Load most-significant byte of count into Counter 0 at I/O port address base+0.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly, enter the downcount value in BCD if the counter was so programmed.

d. Repeat steps b and c for Counters 1 and 2.

Table 3-6. Typical PIT Control Word Subroutine

```
;INTTMR INITIALIZES COUNTERS 0,1,2.
;COUNTERS 0 AND 1 ARE INITIALIZED AS SQUARE WAVE GENERATORS.
;COUNTER 2 IS INITIALIZED AS PROGRAMMABLE ONE-SHOT.
;ALL THREE COUNTERS ARE SET UP FOR 16-BIT OPERATION.
;DESTROYS-AL.
        PUBLIC  INTTMR
INTTMR: MOV     AL,36H          ;MODE CONTROL WORD FOR COUNTER 0
        OUT     BASAD+3,AL
        MOV     AL,76H          ;MODE CONTROL WORD FOR COUNTER 1
        OUT     BASAD+3,AI
        MOV     AL,B2H          ;MODE CONTROL WORD FOR COUNTER 2
        OUT     BASAD+3,AL
        RET
        END
```

Table 3-7. Typical PIT Count Value Load Subroutine

```
;LOAD0 LOADS COUNTER 2 FROM CX, CH IS MSB, CLK IS LSB
;USES-D,E. DESTROYS—AL.
        PUBLIC  LOAD0
LOAD0:  MOV     AL,C            ;GET LSB
        OUT     BASAD+2,AL
        MOV     AL,CH           ;GET MSB
        OUT     BASAD+2,AL
        RET
        END
```

3-45. OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency divide/ratio selection, and interrupt timer counter selection.

3-46. COUNTER READ. There are two methods that can be used to read the contents of a particular counter. The first method involves a simple read of the desired counter. The only problem encountered when using this method is that the count cannot be stablized for reading; the gate input cannot be controlled.

The second method allows the counter to be read on-the-fly. The recommended procedure is to use a mode control word to latch the contents of the count register. This ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

If a counter is read on the fly, it is mandatory to complete the read procedure. That is, if two bytes were programmed to the counter, then two bytes must be read before any other operations are performed with that counter.

To read the count of a particular counter, proceed as follows (a typical counter read subroutine is given in Table 3-8):

a. Write counter register latch control word (Figure 3-9) to port base+3. The control word specifies the desired counter and selects the counter latching operation.

b. Perform a read operation of the desired counter. (Refer to Table 3-1 for counter addresses.)

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes, read in the order specified.

Table 3-8. Typical PIT Counter Read Subroutine

```
;READ1 READS COUNTER 2 ON-THE-FLY INTO CX, MSB IN CH, LSB IN CL.
;DESTROYS-AL.CX.
        PUBLIC  READ1
READ1:  MOV     AL,80H          ;MODE WORD FOR LATCHING COUNTER 2 VALUE
        OUT     BASAD+3,AL
        IN      AL,BASAD+2      ;LSB OF COUNTER
        MOV     CL,A
        IN      AL,BASAD+2      ;MSB OF COUNTER
        MOV     CH,AL
        RET
        END
```

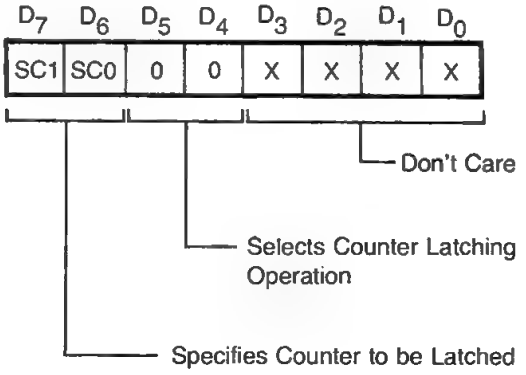


Figure 3-9. PIT Counter Register Latch Control Word Format

3-47. CLOCK FREQUENCY/DIVIDE RATIO SELECTION. The timer input frequency to counters 0 through 2 is 8.00 MHz. The timer input frequency is divided by the counters to generate OUT0, OUT1, and OUT2.

Each counter must be programmed with a count value N. When count value N is loaded into a counter, it becomes the clock divisor. To derive the output frequency (modes 2, 3) or time interval (mode 4) for any given count, use the following formula:

$$\text{Output frequency} = \frac{F}{N}$$

$$\text{Time interval} = \frac{N}{F}$$

Where N = count value
F = 8.000 MHz, the timer clock frequency

3-48. RATE GENERATOR / INTERVAL TIMER. Table 3-9 shows the count values for rate generator operation frequencies. The table also provides the maximum and minimum generator frequencies.

Table 3-9. Rate Generator Frequencies

Baud Rate (bits/sec)	8254 Divide Count		
	Synchronous	Self-Clocking	
64K	125	Tx Clock	32x Clock
56K	143	—	—
48K	167	—	—
19.2K	417	—	—
9600	833	833	26
4800	1667	1667	52
2400	3333	3333	104
1200	6667	6667	208
600	13333	13333	417
300	26667	26667	833
N	8.0×10^6 / N / Counter 0	8.0×10^6 / N / Counter 0	2.5×10^5 / N / Counter 1

NOTE: All numbers are in decimal notation.

3-49. INTERRUPT TIMER. To program an interval timer for an interrupt on terminal count, program the appropriate timer for the correct operating mode (mode 0) in the control word. Then load the count value (N), which is derived by:

Table 3-10 shows the count value (N) required for several time intervals (T) that can be generated for the counters.

N =TF
Where:
N = count value for counter.
T = desired interrupt time interval in seconds.
F = input clock frequency.

Table 3-10. PIT Time Intervals Vs. Timer Counts

T	N
10 uSec	80
100 uSec	800
1000 uSec	8000

NOTES: Count values assume a clock frequency of 8.00 MHz.
Count values (N) are in decimal.

3-50. PROGRAMMING EXAMPLES

The programming sequence for the iSBX 352 board consists of transferring parameters and commands into the 8254-2 PIT and the 8273. The programming examples for the 8273 include an example (Table 3-11) that initializes the 8254-2 PIT and the 8273 device on the iSBX 352 board, an example (Table 3-12) that places the 8273 device into selective receive operation, and an example (Table 3-13) that places the 8273 device into general transmit operation. The examples are written in PL/M and follow the general sequence flowcharted in Figures 3-2 (command phase) and 3-3 (result phase). A more detailed and comprehensive programming example may be found in the section of the *Intel Peripheral Design Handbook* entitled; *Using the 8273 HDLC/SDLC Protocol Controller.*

Table 3-11. 8254-2 and 8273 Initialization Example

This example lists an iSBX 352 board initialization routine that sets up the 8273 and the 8254-2 for operation. The sequence includes a routine to issue a software reset to the 8273. Note that the declare statements in the program are set-up for a host iSBC Microcomputer with a multimodule connector at port address 0FXH.

```
INIT$352: Procedure;
Declare C byte;
Declare CMD73 Literally '0F4H',
Declare PAR73 Literally '0F5H',
Declare RSET73 Literally '0F6H',
Declare TEMP byte;
/*The following table contains the parameters required to initialize the 8723 device for operation. The sequence of
    parameters and the function of the parameters in the table are as follows:
        Number of parameters in command
        Command byte
        Parameter 1
        Parameter 2
        Parameter X. */
DECLARE INIT$73(*) BYTE DATA
        (01H, 64H, 07FH,                    /* Reset one-bit delay, */
                                            /* number of parameters following the command,
                                               command, parameters. */
         01H, 57H, 0FEH,                    /* Select data transfer mode. */
         01H, 91H, 0DH,                     /* Select SDLC, early transmit interrupt, buffered mode, and
                                               flag stream mode. */
         01H, 0A0H, 01H,                    /* Select serial I/O mode and NRZ1 mode. */
         01H, 0A3H, 05H,                    /* Set the RTS (request to send) and DTR (data terminal ready)
                                               bits on the interface to active levels. */
         0FFH);                             /* Last entry in the command/parameter table. */
  /* The following instructions output the 8273 initialization table to the 8273 device. */
        OUTPUT (RSET73) = 01H;              /* Issues the first byte of the software reset to the 8273 device. */
        CALL WAIT$DELAY;                    /* Initiates a 2.5 millisecond delay before issuing the second
                                               byte of the reset to the 8273 device. */
        OUTPUT (RSET73) = 00H;              /* Second byte of software reset. */
```

Table 3-11. 8254-2 and 8273 Initialization Example (Continued)

```
/* The following routines output the contents of the 8273 initialization table to the 8273 device. */
    C=0;
    DO WHILE INIT$73(C) <> 0FFH;
    TEMP = INIT$73(C);
    C=C+1;
    CALL WAIT$CMD;
    OUTPUT (CMD73) = INIT$73(C);
    C=C+$;
    DO WHILE TEMP <> 0;
    CALL WAIT$PAR;
    OUTPUT (PAR73) = INIT$73(C);
    C=C+1;
    TEMP = TEMP-1;
    END;
    END;
    END INIT$352

/*The following instructions contain the parameters required to initialize Counter 0 and Counter 1 of the 8254-2 PIT for
operation as a Square Wave Generator (Mode 3 operation). Note that the parameters CTRL54, CTR54$0, and CTR54$1 can
be equated to the BASADR+3, BASADR+0, and BASADR+1 listed in Table 3-1. */

Declare CTRL54 Literally '0F3H',
Declare CTR54$0 Literally '0F0H',
Declare CTR54$1 Literally '0F1H',

OUTPUT (CTRL54)=36H;                    /* Selects Mode 3 operation for Counter 0. */
OUTPUT (CTR54$0)=TX$BAUD;               /* Sets up the Tx Clock baud rate by outputting low byte and high
                                           byte to 8254-2 PIT.*/
OUTPUT (CTR54$0)=SHR(TX$BAUD,8)         /*

OUTPUT(CTRL54)=76H;                     /* Selects Mode 3 operation for Counter 1. */
OUTPUT (CTR54$1)=TX$BAUD;               /* Sets up the Rx Clock baud rate. */
OUTPUT (CTR54$1)=SHR(TX$BAUD,8)         /*
```

Table 3-12. Configuration of 8273 for Selective Receive Operation

```
SEL$REC$NORM: PROCEDURE(A1,A2);
DECLARE (A1,A2) BYTE;
CALL WAIT$CMD;
OUTPUT(CMD73)=0C1H;                     /* Code for Selective Receive Command. */
CALL WAIT$PAR;
OUTPUT(PAR73)=LENGTH;                   /* Data length parameter, low byte. */
CALL WAIT$PAR;
OUTPUT(PAR73)=SHR(LENGTH,8);            /* Data length parameter, high byte. */
CALL WAIT$CMD;
OUTPUT(CMD73)=A1;                       /* Address field paramter, low byte. */
CALL WAIT$PAR;
OUTPUT(PAR73)=A2;                       /* Address field parameter, high byte. */
END SEL$CON$NORM;

WAIT$CMD: PROCEDURE;
Declare STAT73 Literally '0F4H',
Declare CBSY Literally '80H';
DO WHILE (INPUT(STAT73) AND CBSY) = CBSY;   /* If command is busy, loop until not-busy. */
END;
END WAIT$CMD;

WAIT$PAR: PROCEDURE;
Declare STAT73 Literally '0F4H',
Declare CPBF Literally '20H';
DO WHILE (INPUT(STAT73) AND CPBF) = CPBF;   /* If parameter buffer is not full, loop until all parameters are
                                               received.
                                               */
END
END WAIT$PAR;
```

Table 3-13. Configuration of 8273 for General Transmit Operation

```
TRANS$NORM: PROCEDURE(A1,C1);
DECLARE (A1,C1) byte;
CALL WAIT$CMD;
OUTPUT(CMD73)=0C8H;          /* Issue a General Transmit command code to the 8273 device. */
CALL WAIT$PAR;
OUTPUT(PAR73)=LENGTH;        /* Load the data length parameter to the 8273 device, low byte. */
CALL WAIT$PAR;
OUTPUT(PAR73)=SHR(LENGTH,8); /* Load the data length parameter to the 8273 device, high byte. */
OUTPUT WAIT$PAR;
OUTPUT(PAR73)=A1;            /* Load the Address field parameter for the frame to the 8273
                                device. */

CALL WAIT$PAR;
OUTPUT (PAR73)=C1;           /* Load the Control field parameter for the frame to the 8273
                                device. */

END;
END TRANS$NORM;

   */ Refer to Table 3-12 for a description of the WAIT$CMD and WAIT$PAR subroutines. */
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional overview and a detailed theory of operations for the iSBX 352 Bit Serial Communications Multimodule Board. The iSBX 352 board is a single-wide Multimodule board providing bit serial expansion based around Intel's HDLC/SDLC Serial Controller device (the 8273) and the 8254-2 Programmable Interval Timer (PIT). The iSBX 352 board supports a subset of the RS232C and RS422/449 standard interfaces.

The operations performed on the iSBX 352 Bit Serial Communications Multimodule Board are mainly the work of the 8273 HDLC/SDLC Programmable Communication Protocol Controller and the 8254-2 Programmable Interval Timer. The following paragraphs contain some general information on the internal operations performed by the 8273; more detailed information can be obtained in the *Intel Component Data Catalog* and in the *8273 Application Note, AP36.*

4-2. FUNCTIONAL DESCRIPTION

Figure 4-1 shows a functional block diagram of the iSBX 352 board. As shown, the board can be divided into the following sections:

* iSBX Bus Interface
* Serial Controller
* Clock Generator
* Bit Rate Generator
* Serial Interface
* Chip Select Logic

Operating considerations for each section are outlined in the following paragraphs.

4-3. iSBX BUS INTERFACE DESCRIPTION

Programmed control of the iSBX 352 Bit Serial Communication Multimodule Board is achieved by controlling the signals that interface to and from the iSBX 352 board via the iSBX bus connector. The

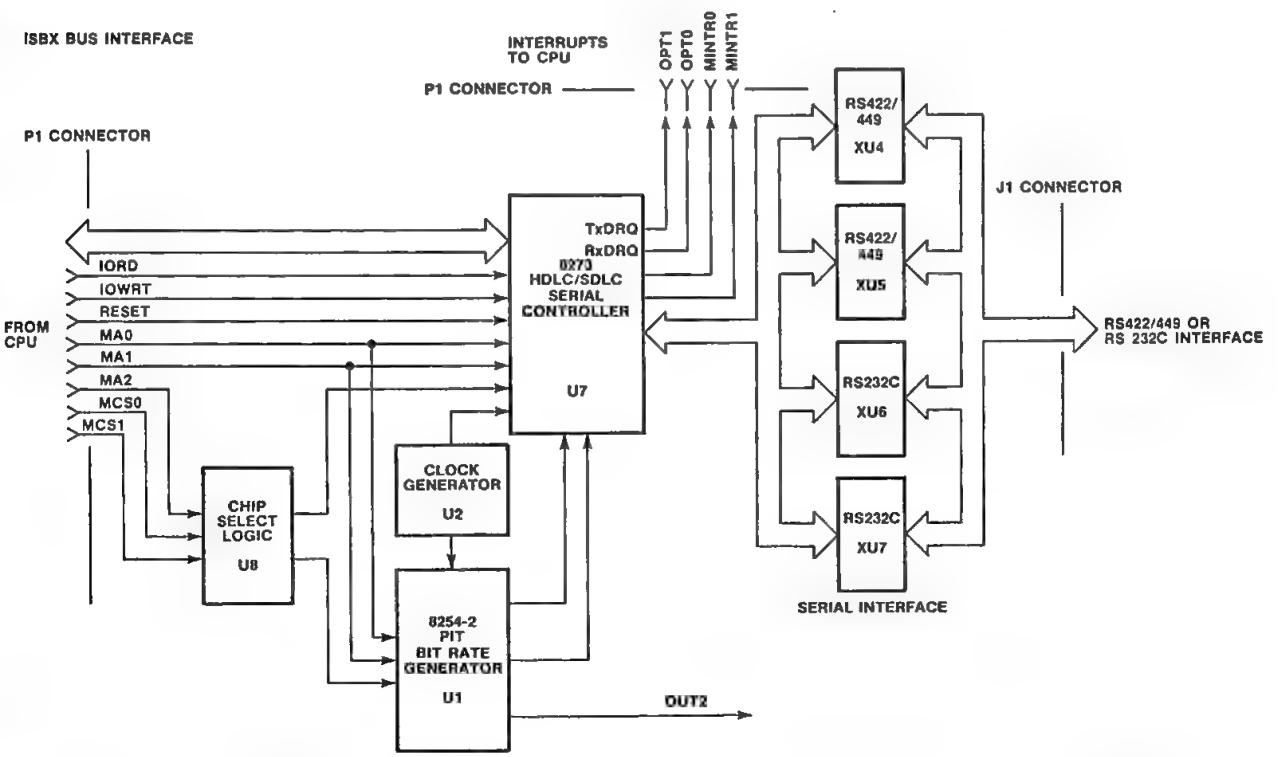


Figure 4-1. iSBX 352™ Bit Serial Communication Multimodule Board Block Diagram

iSBX bus signals that interact with the iSBX 352 board and their functions are detailed in the following paragraphs. Refer to table 2-4 for a listing of the iSBX Bus interface pin assignments.

RESET (Reset)- This active HIGH signal, when asserted to the iSBX 352 board via connector P1 pin-5, holds the 8273 device on the iSBX 352 board in an idle state. When the RESET signal is removed from the interface, the 8273 device remains in an idle state until a command is received from the host iSBC microcomputer. All modem output interface signals are forced HIGH during RESET. The 8273 requires a minimum RESET signal duration of 2.5 uS.

MD0-MD7 (Bidirectional data bus)- These eight, active HIGH, bidirectional data lines provide a means of transferring commands, parameters, status, and data between the LSI devices on the iSBX 352 board (8273 and 8254-2 PIT) and the CPU on the host iSBC microcomputer.

IORD/ (Read Command)- This active LOW input signal to the iSBX 352 board is generated by the host iSBC microcomputer as a command to the iSBX 352 board to output either data or status via the bidirectional data bus (MD0-MD7) to the host iSBC microcomputer.

IOWRT/ (Write Command)- This active LOW input signal to the iSBX 352 board is generated by the host iSBC microcomputer as a command to the iSBX 352 board to accept data present on the bidirectional data bus. The IOWRT/ signal, on connector P1 pin-13, causes the 8273 device to accept either data or commands into the device from the host iSBC microcomputer.

MCS0/ and MCS1/ (Chip Selects)- These active LOW input signals to the iSBX 352 board enable the response to either an input or an output instruction executed on the host iSBC microcomputer board.

MA0, MA1, MA2 (Function Selectors)- These active HIGH inputs from the host iSBC microcomputer select the register in the 8273 that is to be accessed during the operation performed on the iSBX 352 board.

OPT0 (Receiver Data Transfer Request or PIT Counter 2 Output)- This active HIGH output signal from the 8273 device on the iSBX 352 board provides an indication to the host iSBC microcomputer that the receive logic within the 8273 device requires data transfer service. The OPT0 signal may be used as a timed interval interrupt request generator when connected to the output of Counter 2 of the PIT.

OPT1 (Transmitter Data Transfer Request)- This active HIGH output from the iSBX board provides the Transmitter Data Transfer Request signal from the 8273 device to the host iSBC microcomputer. The signal is intended to be used as an interrupt request for the host iSBC microcomputer.

MINTR0 (Transmitter Interrupt)- This active HIGH output from the 8273 device on the iSBX 352 board provides the host iSBC microcomputer with an interrupt request signal whenever the transmitter portion of the 8273 requires service.

MINTR1 (Receiver Interrupt)- This active HIGH output from the 8273 device on the iSBX 352 board provides the host iSBC microcomputer with an interrupt request signal whenever the receiver portion of the 8273 requires service.

4-4. SERIAL CONTROLLER

Serial data transfer control is provided via the 8273 Programmable HDLC/SDLC Protocol Controller which interfaces the parallel iSBX Bus to the serial channel. During a transmit sequence, the 8273 accepts data and commands from the iSBX Bus interface, translates and formats the data into HDLC/SDLC protocol formats, generates the required RS232C or RS449 interface control signals, and passes the data onto the serial channel. During a receive operation, the 8273 accepts data and status from the serial channel, generates the required RS232C or RS449 interface control signals, translates and formats the data into a parallel binary format, and passes the data onto the parallel iSBX Bus interface.

The Receiver Clock (RxC) for the 8273 is jumper configurable to originate from one of two sources; either from the serial interface (RxC) for synchronous operation or from the phase-lock-loop internal to the 8273 in self-clocking applications.

All functions of the 8273 are supported by the iSBX 352 board except for some of the General Purpose Input and General Purpose Output port signals that provide modem control from the 8273. The PA2 input port provides the Data Terminal Ready (DTR) signal and the PB2 output port provides the Data Set Ready (DSR) signal required in either an RS232C or an RS422/449 interface. The remaining I/O lines on the 8273 (PA3, PA4, PB1, PB3, flag detect, and PB4) are not required to perform the data transfer.

4-5. CLOCK GENERATOR LOGIC

The clock generator on the iSBX 352 board supplies the reference timing signals required by the bit-rate generator and the serial controller. The major logic components of the clock generator circuitry are a crystal oscillator (Y1) and a clock divider (U2). The

crystal oscillator provides the basic clock source of 24.000 MHz on the iSBX 352 board. This frequency is divided by 6 in the 8284A to provide a 4.000 MHz basic clock (PCLK from pin-2) for the 8273, and divided by 3 to provide an 8.000 MHz basic clock (CLK from pin-8) to the bit-rate generation logic (the 8254-2 PIT). The 8.000 MHz clock input to the 8254-2 allows for user selection of a wide range of baud rates from the PIT.

4-6. BIT-RATE GENERATOR LOGIC

The Bit-Rate Generator, consisting of the 8254-2 PIT, provides the serial data clocks (the TxC clock and the 32x clock) required by the 8273 for performing the required data transfer operations. Two of the timers in the 8254-2 PIT (timer 0 and timer 1) are dedicated to providing the 2 serial bit-rate clocks required by the 8273. As such, they must be programmed for operation in Mode 3 (square wave generator), as defined in the *Component Data Catalog*. The third timer, Counter 2, in the 8254-2 may be initialized for operation in any mode required for the application. The iSBX 352 board contains jumper provisions for passing the output of Counter 2 to the host iSBC microcomputer if required. The output from Counter 2 (OUT2) can be connected via jumpers to the Option line (OPT0) on the iSBX bus interface.

NOTE

If NRZI encoding and decoding is required in the application, the serial bit-rate generated from Timer 1 of the 8254-2 PIT must be programmed to provide an output clock with a frequency of 32 times the serial receive data bit-rate (32x clock); the phase-locked-loop circuitry within the 8273 requires the 32x clock.

4-7. SERIAL INTERFACE

The buffering required to convert the TTL signals from the 8273 to either RS232C or RS422 interface levels is accomplished through the use of two sets of linear line driver/receiver chips. Configuration of the serial interface (J1) on the iSBX 352 board as an RS232C interface requires installation of an MC1488 and an MC1489 line driver in sockets XU6 and XU3, respectively, and no line driver/receivers in sockets XU4 and XU5. Configuration of the serial interface (J1) as an RS422 interface (the as-shipped configuration) requires an MC3486 and an MC3487 line driver in sockets XU4 and XU5, respectively, and no line driver/receivers in sockets XU3 and XU6.

CAUTION

The iSBX 352 board cannot contain both sets of line driver/receivers in their respective sockets at the same time without causing damage to the iSBX 352 board.

4-8. CHIP SELECT LOGIC

The chip select logic on the iSBX 352 board decodes the MCS0/, MCS1/, and MA2 signals from the iSBX Bus interface to generate the four different chip-select states required by the iSBX 352 board to operate the 8273 and the 8254-2 PIT. The states are shown in Table 4-1. When both chip select terms from the iSBX bus interface are either active or inactive, the iSBX 352 board can be considered "not selected". The relationship between the interface signals found on the iSBX Bus interface and the port address decodes for the 8273 is listed in Table 4-2.

Table 4-1. Chip Select Decodes

MCS1/ State	MCS0/ State	MA2 State	Function Performed On Board
MCS1/=1	MCS0/=1	MA2 = X	None; board remains inactive.
MCS1/=0	MCS0/=1	MA2 = 0	Chip select logic generates an input pulse to the Receiver DMA Acknowledge input pin on the 8273; this indicates to the 8273 that receive data is being read from the 8273 by the host iSBC microcomputer.
MCS1/=0	MCS0/=1	MA2 = 1	Chip select logic generates an input pulse to the Transmitter DMA Acknowledge input pin on the 8273; this indicates to the 8273 that transmit data is being written to 8273 by the host iSBC microcomputer.
MCS1/=1	MCS0/=0	MA2 = 0	Chip select logic generates an input pulse to the 8254-2 PIT, selecting the device for an I/O operation on MD0 through MD7.
MCS1/=1	MCS0/=0	MA2 = 1	Chip select logic generates an input pulse to the 8273, selecting the device for an I/O operation on MD0 through MD7.

Table 4-2. Command Decode Signal Operation

Port Addr	MA1	MA0	TxDACK/ U8 pin 12	RxDACK/ U8 pin 13	CS U8 pin 10	IORD/	IOWRT/	Register
X4	0	0	1	1	0	1	0	Command
X4	0	0	1	1	0	0	1	Status
X5	0	1	1	1	0	1	0	Parameter
X5	0	1	1	1	0	0	1	Result
X6	1	0	1	1	0	1	0	RESET
X6	1	0	1	1	0	0	1	TxINT Result
X7	1	1	1	1	0	1	0	—
X7	1	1	1	1	0	0	1	RxINT Result
Y0	X	X	0	1	1	1	0	Transmit Data
Y4	X	X	1	0	1	0	1	Receive Data

Notes:

4-9. DETAILED CIRCUIT ANALYSIS

The following paragraphs describe circuit operations on the iSBX 352 board including transmit, receive, and interrupt operation. Refer to the specification sheet for the 8273 device if you require more information.

4-10. RECEIVE OPERATION REQUIREMENTS

Figure 4-2 shows a typical Receive operation for an iSBX 352 board. The figure shows an example of error-free frame reception. When the receive operation begins, the 8273 sends out the Beginning flag, the Address field, the Control field, and then begins transferring the Information fields. After the Information fields, the Frame Check Sequence bytes and the Ending flag are transferred. To generate the Address field and Control field data interrupts, the 8273 must be operating in the non-Buffered Mode; refer to the Set Operating Mode command for more information. The figure shows the relationship between the data interrupts and the Receiver Results interrupts.

4-11. TRANSMIT OPERATION REQUIREMENTS

Figure 4-3 shows a typical Transmit operation for an iSBX 352 board. The figure shows three examples of frame transmit; one showing an error-free transfer, one showing operation of the Early Transmit Interrupt feature, and one showing a Clear To Send signal failure during a frame. The format of the frame for the transmit operation is basically the same for all three examples; the 8273 sends out the Beginning flag, the Address field, the Control field, and then begins transferring the Information fields. After the Information fields, the Frame Check Sequence bytes and the Ending flag are transferred. To generate the Address field and Control field data interrupts, the 8273 must be operating in the non-Buffered Mode; refer to the Set Operating Mode command for more information. The figure shows the relationship between the data interrupts and the Transmitter Results interrupts.

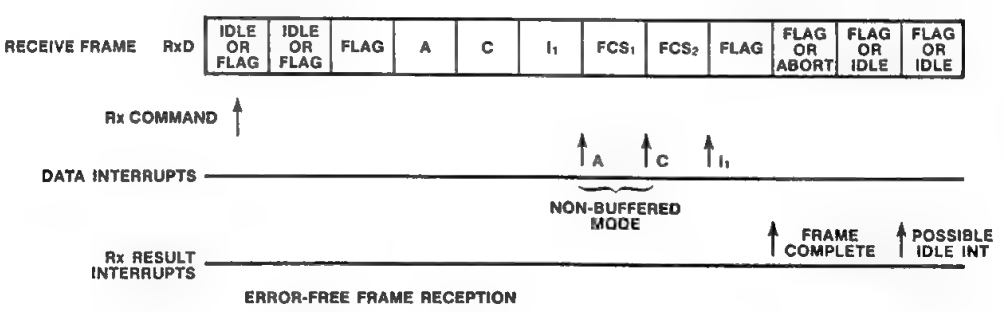


Figure 4-2. Receiver Timing Diagram

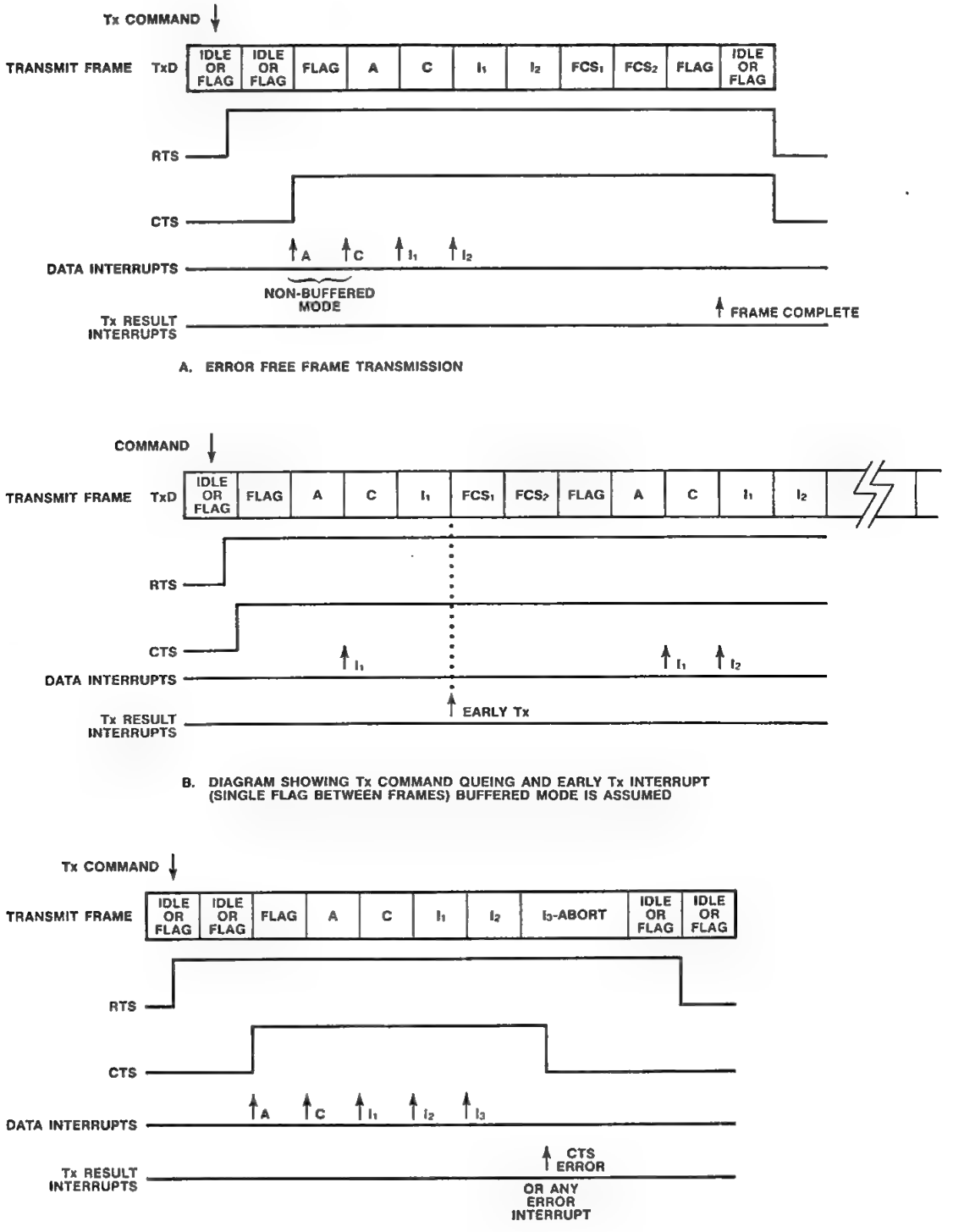


Figure 4-3. Transmit Timing Diagrams

4-12. INTERRUPT OPERATION

The iSBX 352 Bit Serial Communications Multimodule Board is designed to operate on a host iSBC microcomputer board that provides service on either a polling process or an interrupt request/acknowledge process. True data transfers between the host iSBC microcomputer and the iSBX 352 board are not supported. Four interrupts may be generated by the iSBX 352 board to the host iSBC microcomputer; the Transmitter Interrupt Request signal (TxINT), the Receiver Interrupt Request signal (RxINT), the Transmitter Data Transfer Request Interrupt signal (TxDRQ), and the Receiver Data Transfer Request Interrupt signal (RxDRQ) are output from the Multimodule board as MINTR0, MINTR1, OPT1, and OPT0, respectively. Interrupt operation is described in the following paragraphs.

To request a data transfer interrupt, the iSBX 352 board raises the appropriate option line. The host iSBC microcomputer passes a byte of data to the iSBX 352 board via generation of the TxDACK signal and a WRITE command to port address Y0 or Y4 (if for a transmit data interrupt). The combination of the Receive Data Transfer Acknowledge (RxDACK) signal and the READ command causes the 8273 on the iSBX 352 board to transfer data on MD0 through MD7 independent of the condition of the chip select signal (U8 pin-10).

The interrupt lines (MINTR0 and MINTR1) from the iSBX 352 board provide for a polling host iSBC microcomputer a direct reflection of the status of the 8273 device. The MINTR0 signal is a result of the 8273's generation of the TxINT signal, providing an indication of the status of the transmitter portion of the 8273 device. The MINTR1 signal is a result of the 8273's generation of the RxINT signal, providing an indication of the status of the receiver portion of the 8273 device. Both interrupt signals are active HIGH and generated with the intention of relieving the host iSBC microcomputer of the task of polling the iSBX 352 board to determine if the 8273 requires service.

When an interrupt request is generated on either MINTR0 or MINTR1, the interrupt request remains active until all associated interrupt results in the 8273 have been read or until a data transfer is performed. Data request interrupts are separated from result interrupt requests by the condition of bit 2 of the Status Register in the 8273. The state of bit 2 of the Status Register (internal to the 8273) also affords the host iSBC microcomputer the means to poll the iSBX 352 board for servicing, if the configuration requires that no interrupts be used.

4-13. RECEIVE INTERRUPTS. The type of receive interrupt generated by the 8273 is determined by inspecting the Receive Interrupt Code (RIC) byte (the first byte) of the RxIR Register. Table 4-3 shows the various interrupt codes and provides an idea of when each interrupt is generated.

On sensing an interrupt signal from the iSBX 352 board, the host iSBC microcomputer should perform the following functions:

1) Read the contents of the Status Register internal to the 8273 device; accessed at port address X4.
2) Read the results of the operation from either the Transmit Interrupt Result (TxIR) Register on a transmit operation or from the Receive Interrupt Result (RxIR) Register on a receive operation. The RxIR Register provides up to five bytes of information depending on the type of operation performed. Refer to the section of Chapter 3 dealing with status for more detailed information.

The operation of the 8273 device is such that it generates a received frame interrupt on detecting the Ending flag of a frame. Then, 15 bit-times later if there is no subsequent frame, the 8273 generates an idle line detect interrupt. If a condition occurs requiring generation of another interrupt before the host iSBC microcomputer has finished reading the results of the first interrupt, the second interrupt is generated after the current result phase is completed; that is, after the RIC byte is read, the byte is overwritten and the remaining bytes of the RxIR Register remain unchanged. This procedure provides only a one byte interrupt result for the idle line detect interrupt. The contents of the RIC status byte for the second interrupt reflect a Receiver Interrupt Overrun error (bit code 00001011).

4-14. TRANSMIT INTERRUPTS. The type of transmit interrupt generated by the 8273 is determined by inspecting the TIC byte in the TxIR Register. Table 4-2 shows the various interrupt codes and provides an idea of when each transmit interrupt is generated.

On sensing a transmit interrupt signal from the iSBX 352 board, the host iSBC microcomputer should perform the following functions:

1) Read the contents of the Status Register internal to the 8273 device; accessed at port address X4.
2) Read the results of the operation from the Transmit Interrupt Result (TxIR) Register on a transmit operation. The TxIR Register provides one byte of information defining the interrupt.

Refer to the section of Chapter 3 dealing with status for more detailed information.

3) If high-speed (48 to 64K baud) full-duplex operation is required on the iSBX 352 board, you must issue Port Access and Receive type commands to the 8273. Both types of commands begin and/or end with either the transmitter or the receiver portion of 8273 inactive; failure to inactivate one or the other creates internal 8273 operating contentions that can cause a substantial degredation in the operating speed of the board.

Table 4-3. Decodes For The RIC Byte Of The RxIR Register

RIC Bit Code	Reason for Interrupt Generation	Comments
***00000	A1 match or General Receive	Indicates error free reception of the frame.
***00001	A2 match	Indicates error free reception of the frame.
00000011	CRC Error	Indicates that the frame was received in the proper format, however, the generated and the frame-internal FCS characters did not match.
00000100	Abort Detect	Indicates that the receiver detected an abort character in the data stream.
00000101	Idle Detect	Indicates that 15 consecutive 1-bits are detected on the data line.
00000110	EOP Detect	Indicates that the receiver detected an EOP character in the data stream; must be enabled via Set Operating Mode command.
00000111	Frame Length less than 32 bits	Indicates that less than 32 bits (the minimum number of data bits in a frame) were received.
00001000	DMA Overrun	Indicates that the DMA controller is too slow in extracting data from the 8273; the RxDACK/ signal is not returned to the 8273 before the next byte is received.
00001001	Memory Buffer Overflow	Indicates that the number of bytes of data received is larger than the number of bytes specified by the B0 and B1 parameters in the receive command.
00001011	Receive Interrupt Overrun	Indicates that the systems interrupt response and servicing speed is insufficient to keep pace with the data transfer speed.

NOTE: XXX is the number of bits received. Refer to Figure 3-6 for more information.

Table 4-4. Decodes For The TIC Byte Of The TxIR Register

TIC Bit Code	Reason for Interrupt Generation	Comments
00001100	Early Transmitter Interrupt	Generated after the last data transfer to the 8273 if an early interrupt is called for in the Set Operating Mode command.
00001101	Frame Tx Completed	Generated at the detection of the Ending flag to indicate a completed protocol on the transmitted frame.
00001110	Data Transfer Underrun	Generated when the DMA controller does not pass data to the transmitter in time to be transmitted in the frame; the transmitter portion of the 8273 performs an automatic abort.
00001111	Clear To Send Error	Generated when the Clear To Send (CTS) signal drops inactive during a frame transmission.
00010000	Abort Completed	Generated when an abort command is issued to the transmitter; no abort completed status is generated for the automatic abort generated by the 8273.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, and service and repair assistance instructions for the iSBX 352 Bit Serial Communications Multimodule Board.

5-2. SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacing the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Offices or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.
b. Complete part number of the product (including dash number and revision level). This number is usually silk-screened onto the board.
c. Serial number of product. This number is usually stamped on the board.
d. Shipping and billing addresses.
e. Purchase order number for billing purposes if your warranty has expired.
f. Information on extended warranty agreements, if applicable.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

All U.S. locations, except Alaska, Arizona & Hawaii:

(800) 528 - 0595

All other locations: (602) 869 - 4600

TWX Number: (910) 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclosed in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5-3. PARTS LIST

Table 5-1 provides a list of replaceable parts for the Multimodule board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column of Table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML". every effort should be made to procure these parts from a local (commercial) distributer.

5-4. SERVICE DIAGRAMS

The parts location diagram and schematic diagram for the iSBX 352 board are provided in Figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., IORD/) is active LOW. Conversely, a signal mnemonic without the slash (e.g., OPT0) is active HIGH.

Table 5-1. Parts List

Reference Designator	Description	Mfr. Part No.	Mfr. Code	Qty.
U4	IC, RS422 3-state diff. line receiver	MC3486	MOT	1
U10	IC, Hex inverters	74LS04	TI	1
U9	IC, Quad 2-input positive OR gate	74LS32	TI	1
U5	IC, RS422 3-state diff. line driver	MC3487	MOT	1
U8	IC, High Speed 1-of-8 Decoder	8205	INTEL	1
U1	IC, Programmable Interval Timer	8254-2	INTEL	1
U2	IC, Clock Generator and Driver	8284A	INTEL	1
U7	IC, Programmable HDLC/SDLC Controller	8273	INTEL	1
Y1	Crystal, 24 MHz			1
P1	Connector, 36-pin	103109-001	INTEL	1
XU3, XU6	Socket, 14-pin, DIP			2
XU4, XU5	Socket, 16-pin, DIP			2
E1-E27	Wirewrap stake pin	87022-1	AMP	27
	Shorting Plugs	530153-2	AMP	8
R1, R2	Resistor, 510 ohm, 5%, 1/8W	OBD	COML	2
R3	Resistor, 10K, 5%, 1/4W	OBD	COML	1
R4	Resistor, 1K, 5%, 1/4W	OBD	COML	1
C1, C4, C5, C6, C7, C8				
C9	Capacitor, 0.1uF,+80 -20%, 50V, cer.	OBD	COML	7
C10	Capacitor, 4.7uF, ±10%., 10V cer.	OBD	COML	1
U6	IC, Interface, 4x Line Receiver AM	1488 PC	AMD	1
U3	IC, Interface, 4x Line Receiver AM	1489 AN/PC	AMD	1

Table 5-2. Manufacturer Codes

Mfr. Code	Manufacturer	Address
INTEL	Intel Corp.	Santa Clara, CA
MOT	Motorola	Phoenix, AZ
VIK	Viking Connector, Inc.	Chatsworth, CA
AMD	Advanced Microdevices	Santa Clara, CA
AMP	Amp, Inc.	Harrisburg, PA
TI	Texas Instruments	Dallas, TX
OBD	Order by description, any commercial (COML) source	

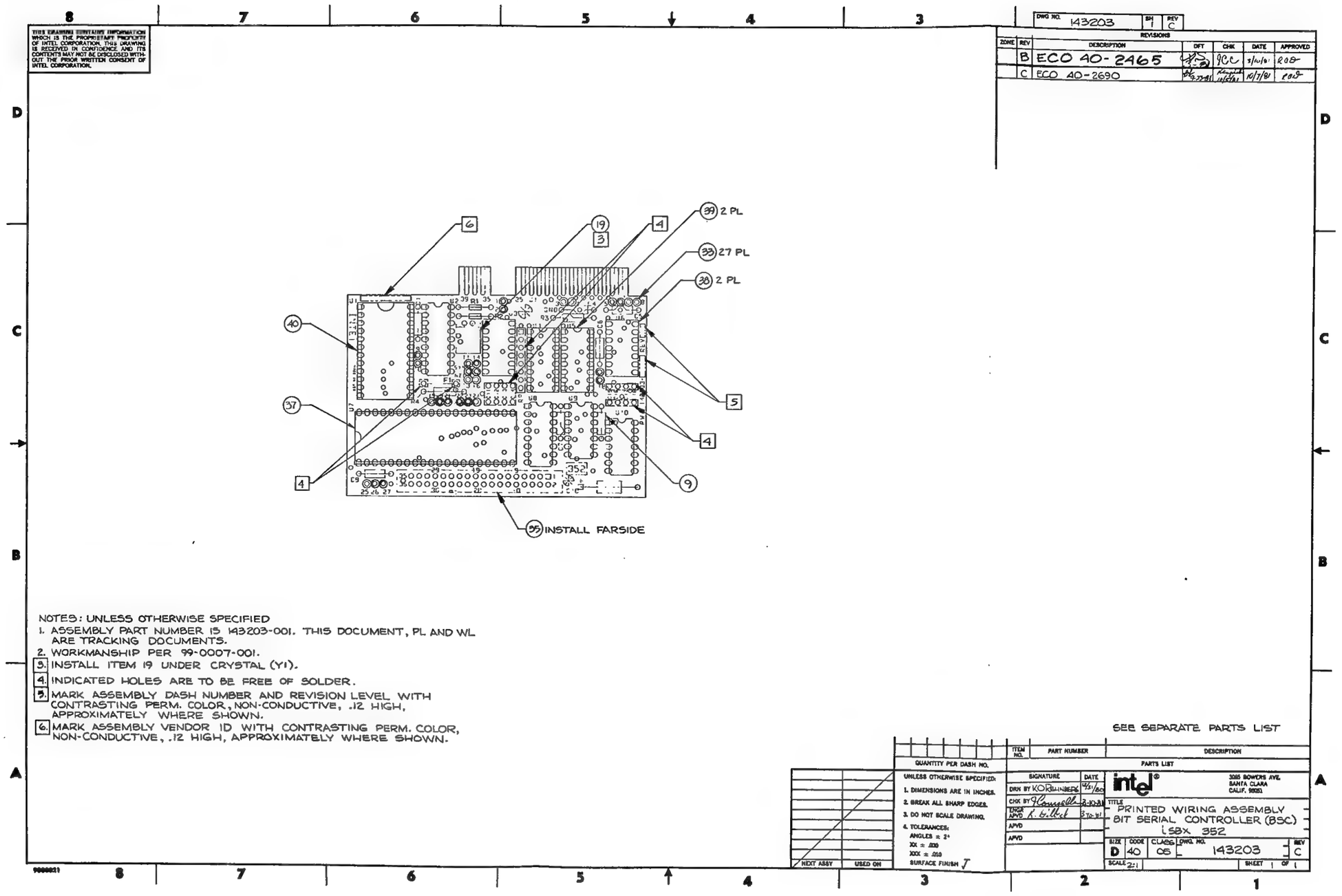
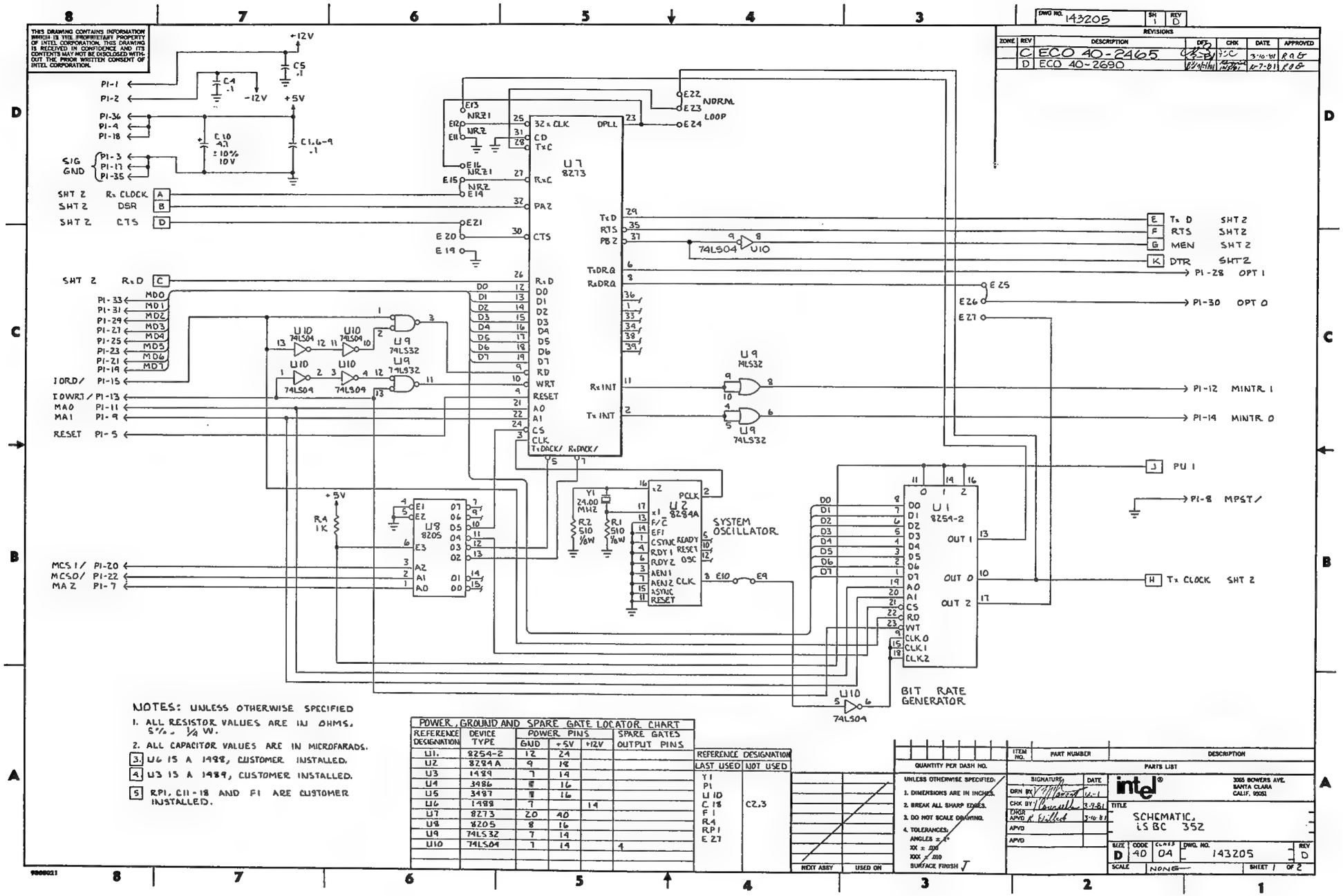


Figure 5-1. iSBX 352™ Bit Serial Communication Multimodule Board Parts Location Diagram



CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Figure 5-2. iSBX 352™ Bit Serial Communication Multimodule Board Schematic Diagram (Sheet 1 of 2)

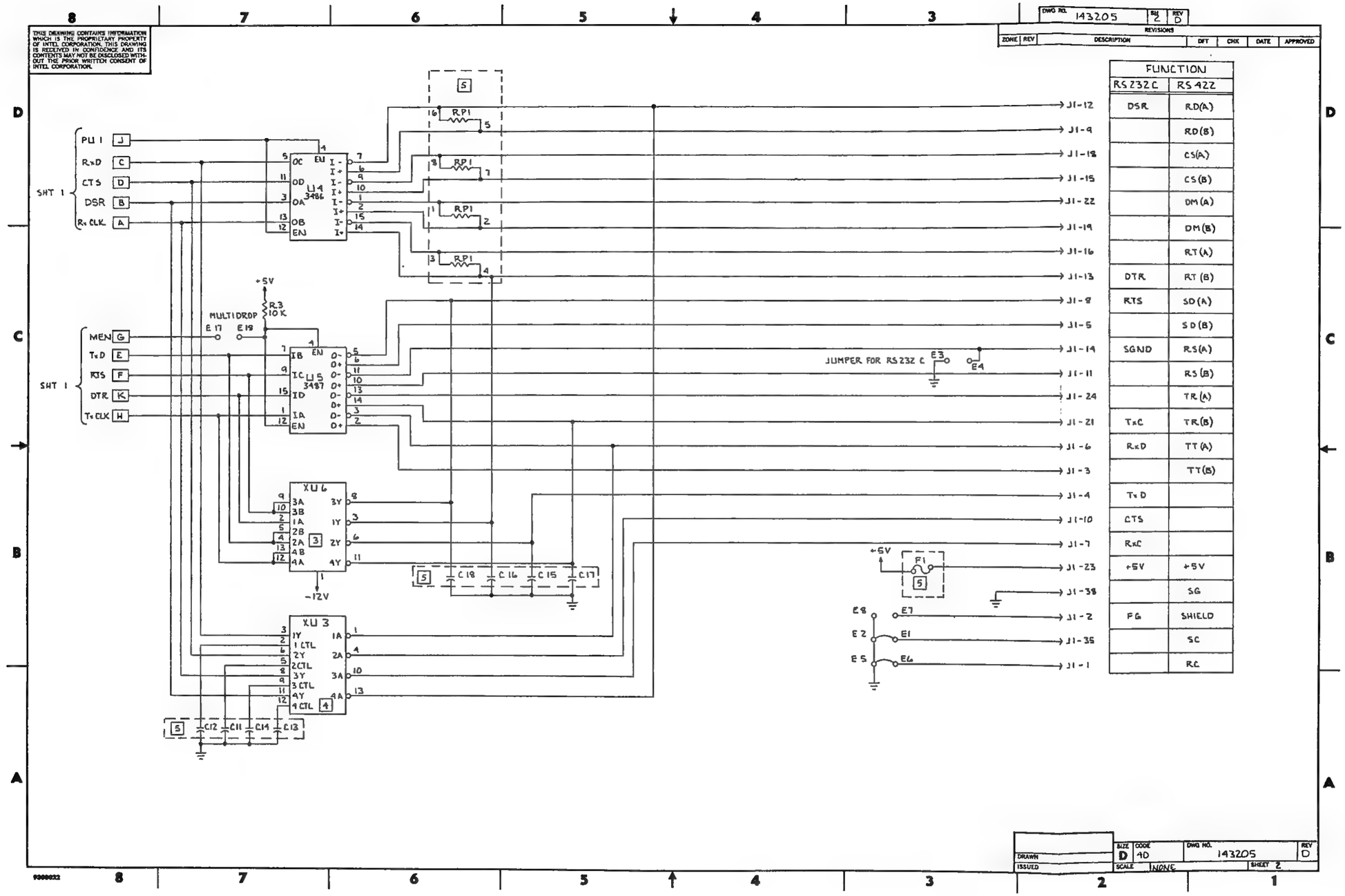


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Figure 5-2. iSBX 352™ Bit Serial Communication Multimodule Board Schematic Diagram (Sheet 2 of 2)

APPENDIX A
MULTIDROP CONSIDERATIONS

A-1. INTRODUCTION

An iSBX 352 Bit Serial Communications Multimodule Board lends itself readily to a multidrop application. This appendix shows an example for configuring an iSBX 352 board for installation into a full-duplex RS422 multidrop application. Some of the line conditioning considerations when configuring the iSBX 352 board for a multidrop system are as follows:

a. You must calculate the value of the bias resistors for installation at the (master/slaves) the system.

b. You must calculate the value of the termination resistors for installation at the farthest slave unit in the system.

The following text discusses the calculation sequence required to determine each of the multidrop application requirements and Figure A-1 shows a configuration example to be used in the explanation. The bias and termination resistors required for the slave and master devices are shown in greater detail in Figures A-2 and A-3.

Figure A-1 shows a typical RS422 full-duplex multidrop configuration which assumes that only one master station is attached to the system and always drives the output lines. Bear in mind that a full-duplex system allows a slave to listen to the data line, and to perform some task in parallel with a task performed on another slave, however, only the selected slave may transmit to the master. In this example, you may include up to 10 slave stations in the system, however, the slaves are under strict program control to output only on command from the master.

You can configure a simpler RS422 multidrop system for half-duplex operation, however, the protocol is more strict. A half-duplex configuration requires two data lines (to carry a differential signal) and a ground line (return) between the master and all slaves in the system. Recall, however, that a major restriction of a half-duplex system is its limitation to communicating in only one direction at a time.

For all practical purposes, the half-duplex system allows no priority for masters and slaves; all units

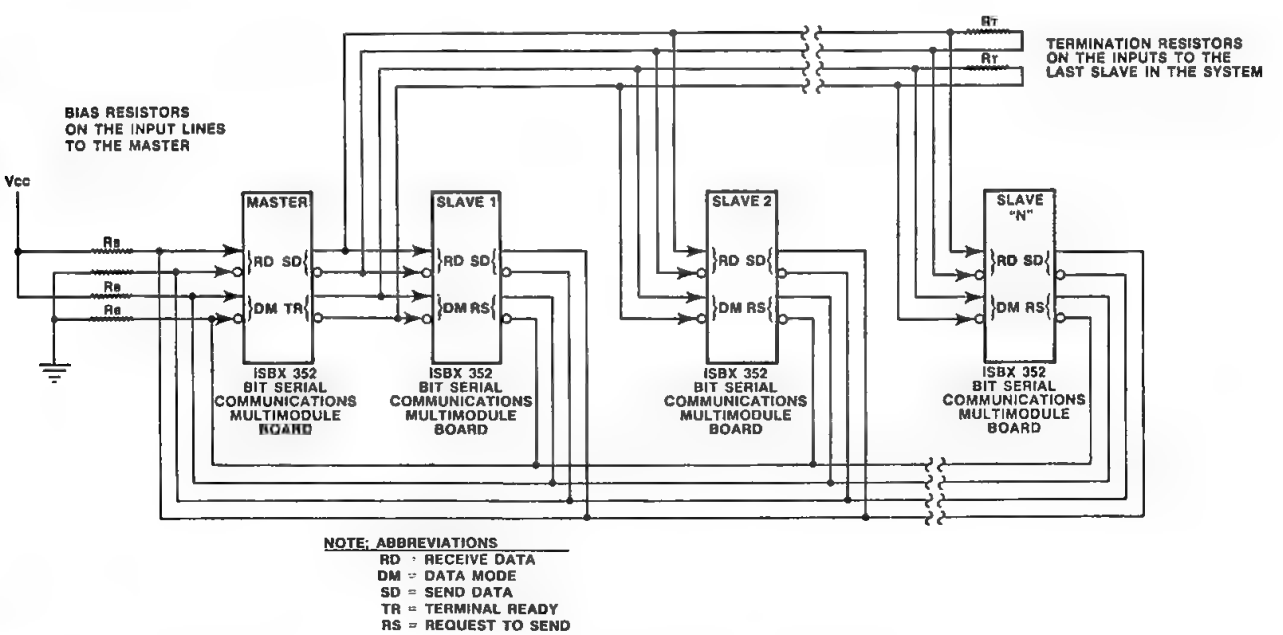


Figure A-1. Full-duplex RS422 Multidrop Configuration Example

may listen to whomever is using the data line. This presents a programming constraint in that the system software protocol for half-duplex operation must be designed to allow only one unit to transmit at any given instant.

A-2. JUMPER CONFIGURATION

The jumper configuration required to operate the iSBX 352 board in a multidrop application consists of installing a jumper from E17 to E18 on all master and slave iSBX 352 boards. Factory configuration of the iSBX 352 board includes no jumper between E17 and E18. The jumper allows the 8273 device to control the state of the output buffers; the buffers can be placed into a high impedance condition for the multidrop application.

A-3. MULTIDROP BIAS RESISTOR REQUIREMENT

In an RS422 multidrop application, it is strongly recommended that the open or floating data lines in the system be biased by means of user supplied bias resistors, as shown in Figure A-2. Without the resistors, the state of a floating line cannot be guaranteed. The exact value of the bias resistors may be calculated only on an individual application basis since the controlling parameters will vary from one application to another. The following procedure steps through an example for calculating the bias resistance required to dissipate the leakage currents encountered in a typical full-duplex RS422 multidrop application. The procedure determines both the best case and the worst case resistor values; any resistor value that satisfies both cases may be installed as a bias resistor.

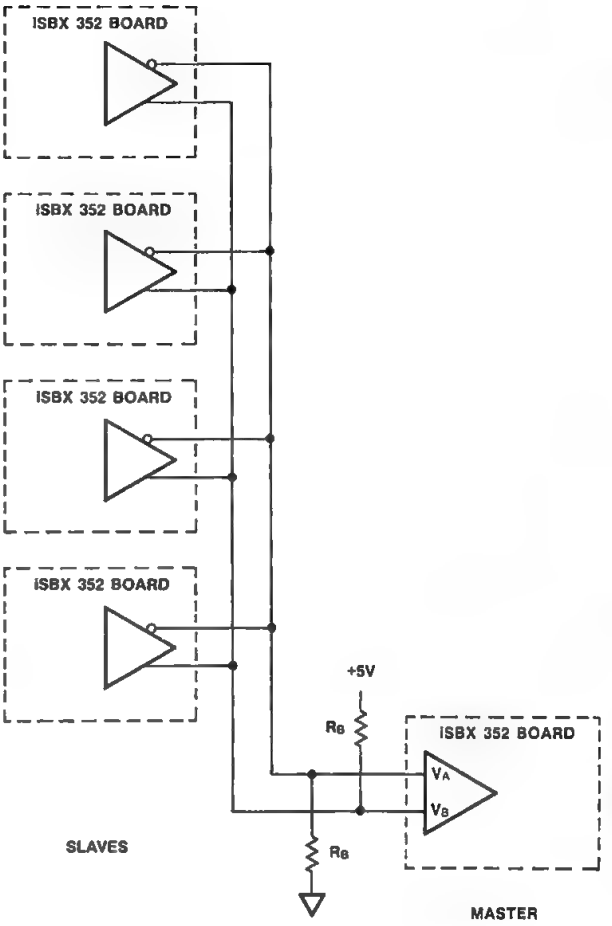


Figure A-2. System Example-Bias Resistors

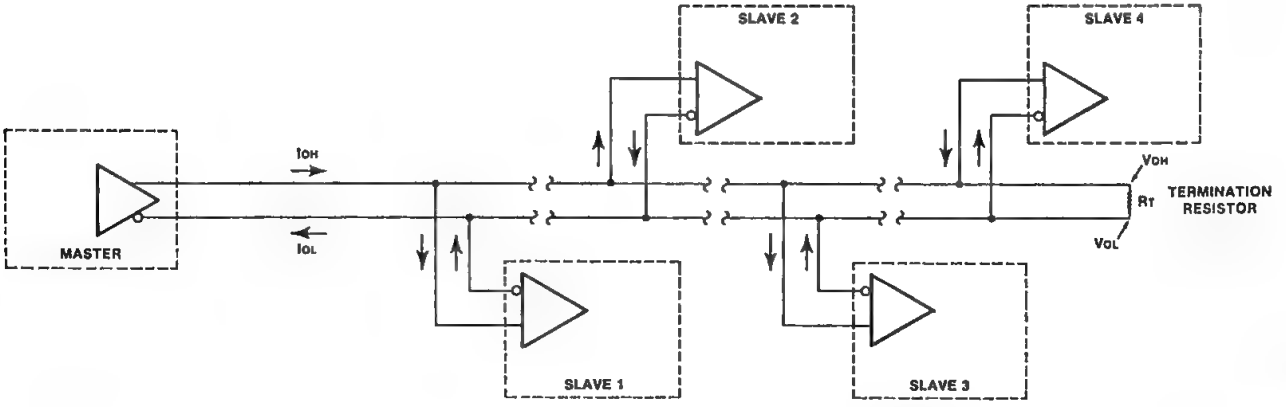
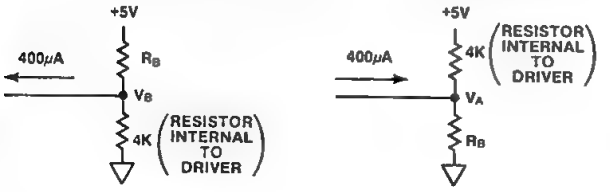


Figure A-3. System Example-Termination Resistors

RESISTANCE CALCULATION WITH BEST CASE CURRENT LOSS

Figure A-2 shows more details of the example presented in Figure A-1. When all four line drivers in the system are in the high impedance state, the current leakage (Va and Vb) into the master is as follows:

1) Assume the following conditions are true for this example:
   * Current (leakage) = 100 uA X 4 devices = 400 uA,
   * Vb is greater than or equal to Va + 0.2 volts,
   * Va = 2.4 volts,
   * Vb = 2.6 volts, and
   * Rb value is equal for both the pull-up and the pull-down resistors in the application.



2) Calculate the required bias resistor value (Rb) with respect to Vb as follows:

   From the diagram,

$$\frac{5.0 \text{ volts} - Vb}{Rb} = 400uA + \frac{Vb}{4K \text{ ohms}}$$

   So,

$$Rb = \frac{5.0 - Vb}{400uA + (Vb/4k)}$$

   In assuming Vb = 2.6 volts, we have

$$Rb = \frac{5.0 - 2.6 \text{ volts}}{400uA + (2.6 / 4)}$$

   Finally, Rb with respect to Vb is

   Rb = 2286 ohms (maximum)

3) Calculate the required bias resistor value (Rb) with respect to Va as follows:

   From the diagram,

$$\frac{Va}{Rb} = 400uA + \frac{5.0 \text{ volts} - Va}{4k \text{ ohms}}$$

   So,

$$Rb = \frac{Va}{400uA + ((5.0 - Va)/4k)}$$

   In assuming Va = 2.4 volts, we have

$$Rb = \frac{2.4 \text{ volts}}{400uA + ((5.0 - 2.4)/4)}$$

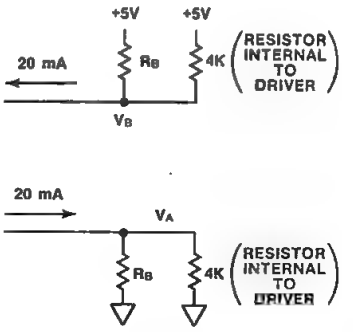
   Finally, Rb with respect to Va is

   Rb = 2286 ohms (maximum).

RESISTANCE CALCULATION WITH WORST CASE CURRENT LOSS

To figure the Rb values when the system is experiencing a worst case drive current, proceed as follows:

1) Assume the following conditions are true for this example:
   * Current (drive) = 5mA X 4 devices = 20mA,
   * Va is greater than or equal to Vb + 0.2 volts,
   * Va = 2.6 volts,
   * Vb = 2.4 volts, and
   * Rb value is equal for both the pull-up and the pull-down bias resistors in the application.



2) Calculate Rb with respect to Vb as for the previous example:

   From the diagram,

$$\frac{5.0 \text{ volts} - Vb}{Rb} + \frac{5.0 \text{ volts} - Vb}{4k \text{ ohms}} = 20mA$$

   So,

$$Rb = \frac{5.0 - Vb}{20mA - ((5.0 - Vb)/4k)}$$

   In assuming Vb = 2.4 volts, we have

$$Rb = \frac{5.0 - 2.4 \text{ volts}}{20mA - (2.6 \text{ V} / 4)}$$

   Finally, Rb with respect to Vb is

   Rb = 134 ohms (minimum)

3) Calculate Rb with respect to Va as follows:

   From the diagram,

$$\frac{Va}{Rb} + \frac{Va}{4k \text{ ohms}} = 20mA$$

   So,

$$Rb = \frac{Va}{20mA - (Va / 4k)}$$

   In assuming Va = 2.6 volts, we have

$$Rb = \frac{2.6 \text{ volts}}{20mA - (2.6V / 4)}$$

   Finally, Rb with respect to Va is

   Rb = 134 ohms (minimum).

In conclusion, we have determined that the value of the bias resistors required for the example application must be greater than 134 ohms and less than 2284 ohms. Any resistor value that satisfies both requirements is acceptable in the application.

A-4. MULTIDROP TERMINATION REQUIREMENT

In an RS422 multidrop application, it is strongly recommended that the inputs to the slave device that is farthest from the master device be terminated as shown in figure A-3 to reduce the line signal reflection. The exact value of the termination resistors can be calculated only on an individual application basis since the contributing parameters will vary from one application to another. The following text shows an example of how to calculate termination resistance for a full-duplex RS422 multidrop application

To calculate the size of the termination resistors required for the example in figure A-1, proceed as follows:

1) Assume the following conditions are true for this example:
   * The system for which we are calculating the value of terminating resistors is configured as shown in figure A-3,
   * Current (leakage) = 100 uA,
   * Input resistance is greater than 4k ohms,
   * V_{ol} = 0.5 volts at I_{ol} = 20 mA,
   * V_{oh} = 2.0 volts at I_{oh} = -20 mA, and
   * The value of Rt is equal for all required termination resistors.

2) Calculate the required termination resistor value (Rt) with respect to Vb as follows:

   Figure the voltage at Rt,

   $Vt = V_{oh} - V_{ol}$

   Substituting the given values,

   Vt = 2.0 volts - 0.5 volts

   So,

   Vt = 1.5 volts

3) Calculate the current drawn by the slaves (Is) as shown. Assuming that Vt at each slave is 4 volts, each slave may draw up to 1mA of current:

   Calculate the current:

   Is = 1.0mA + 1.0mA + 1.0mA + 1.0mA

   So,

   Is = 4.0mA

4) Compute the amount of excess current (Ie) available at Rt. Assuming that Ie = 20mA - Is , the excess current is figured as follows:

   Calculate the excess current,

   Ie = 20mA - Is

   Substituting a value for Is gives

   Ie = 20mA - 4mA

   So,

   Ie = 16mA excess current.

5) Calculate the resistance (Rt) needed to terminate the excess current (Ie) that is available. Use the formula

   $$Rt = \frac{Vt}{Ie}$$

   Substitution gives,

   $$Rt = \frac{2.0 \text{ volts}}{0.016 \text{ amps}}$$

   The termination resistance required is,

   Rt = 125 ohms (minimum)

In conclusion, we have determined that the termination resistance required for the example must not be less than 125 ohms. The actual value selected for the termination resistors should approximate the calculated value; the value should approximate that of the line impedance of the system.

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